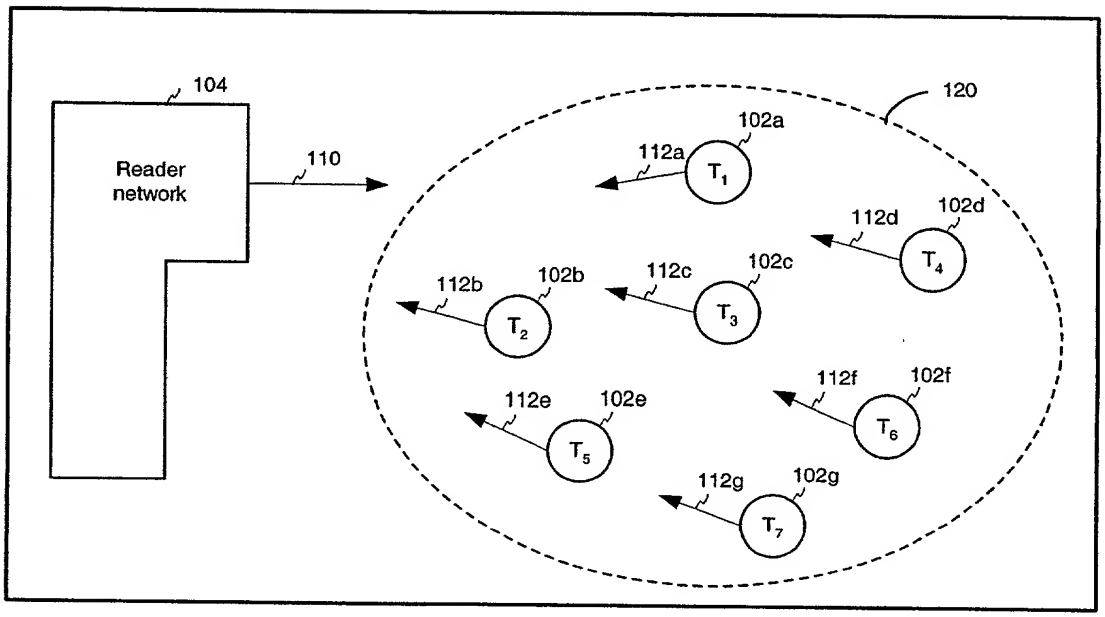

FIG. 1

Reader Network / Site

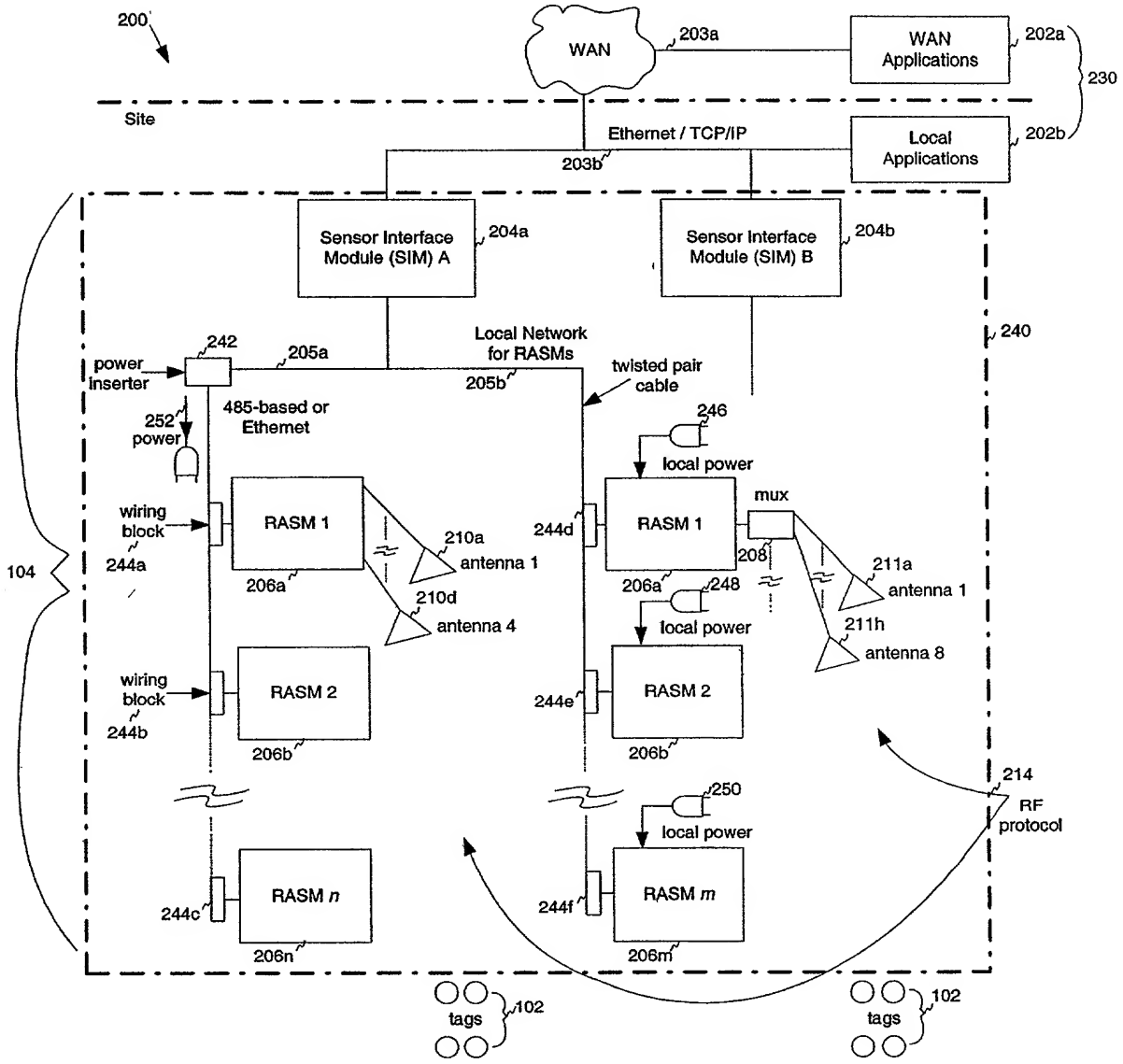

FIG. 2

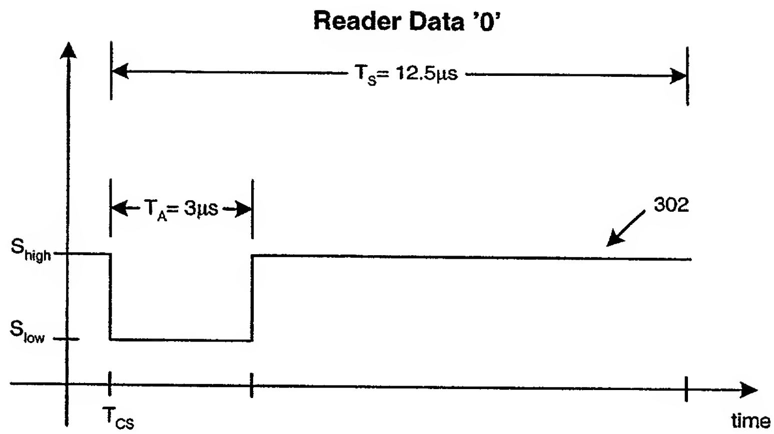

FIG. 3

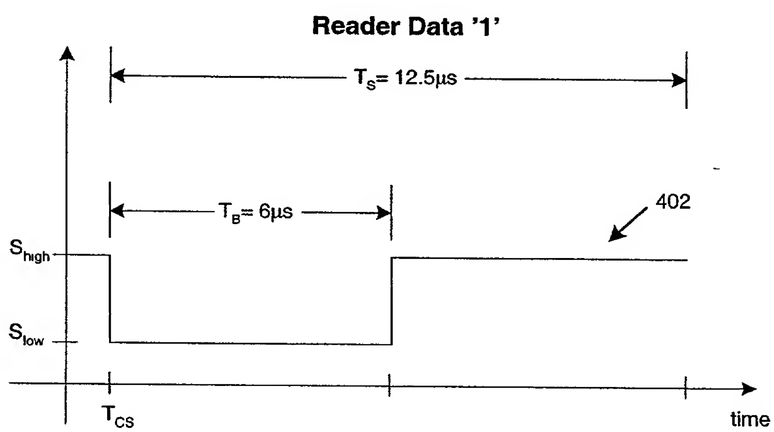

FIG. 4

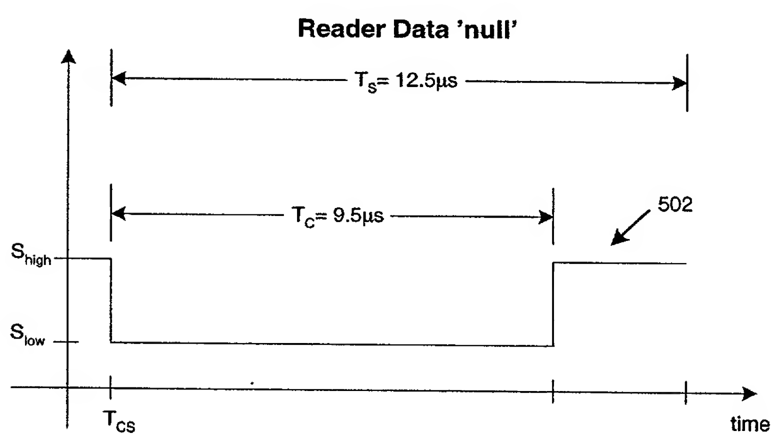

FIG. 5

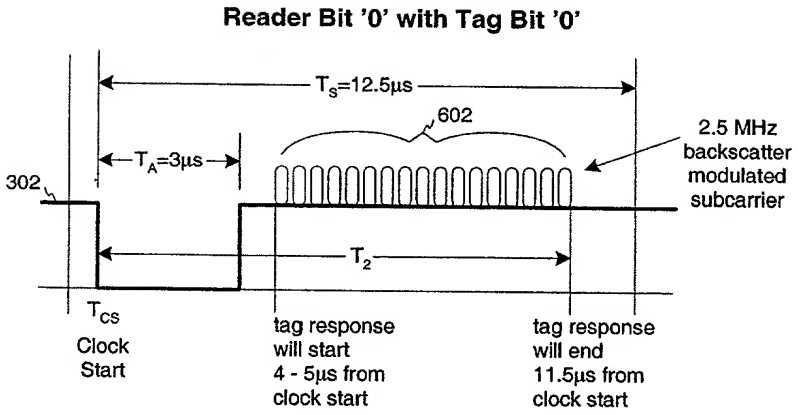

FIG. 6

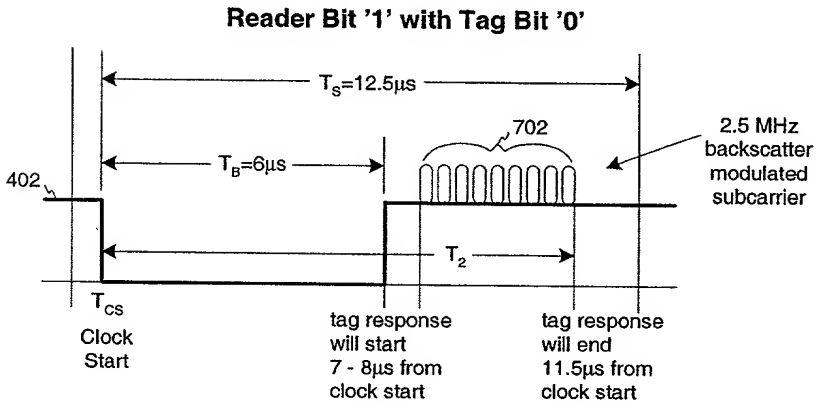

FIG. 7

Reader Bit '0' with Tag Bit '1'

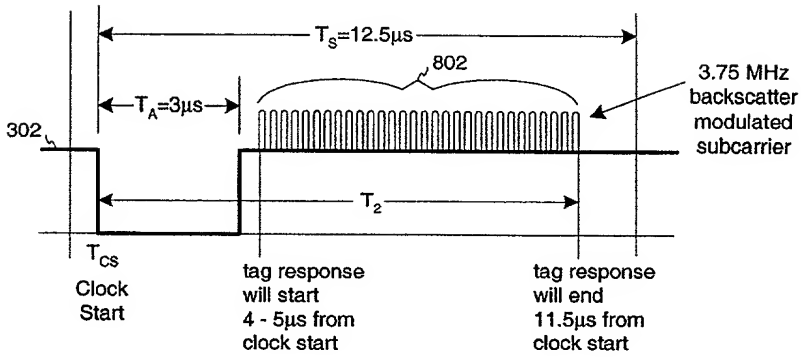

FIG. 8

Reader Bit '1' with Tag Bit '1'

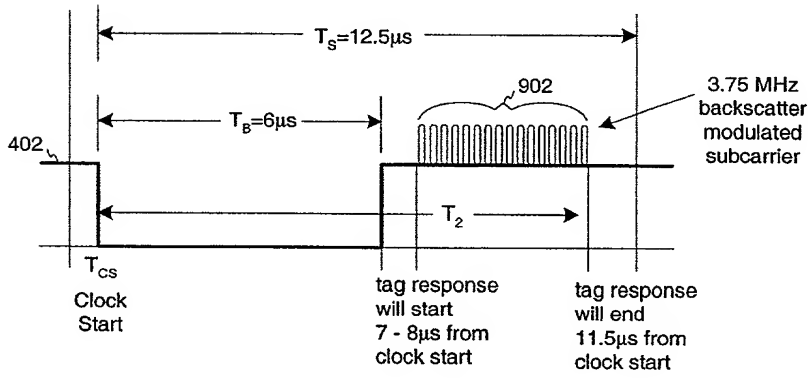

FIG. 9

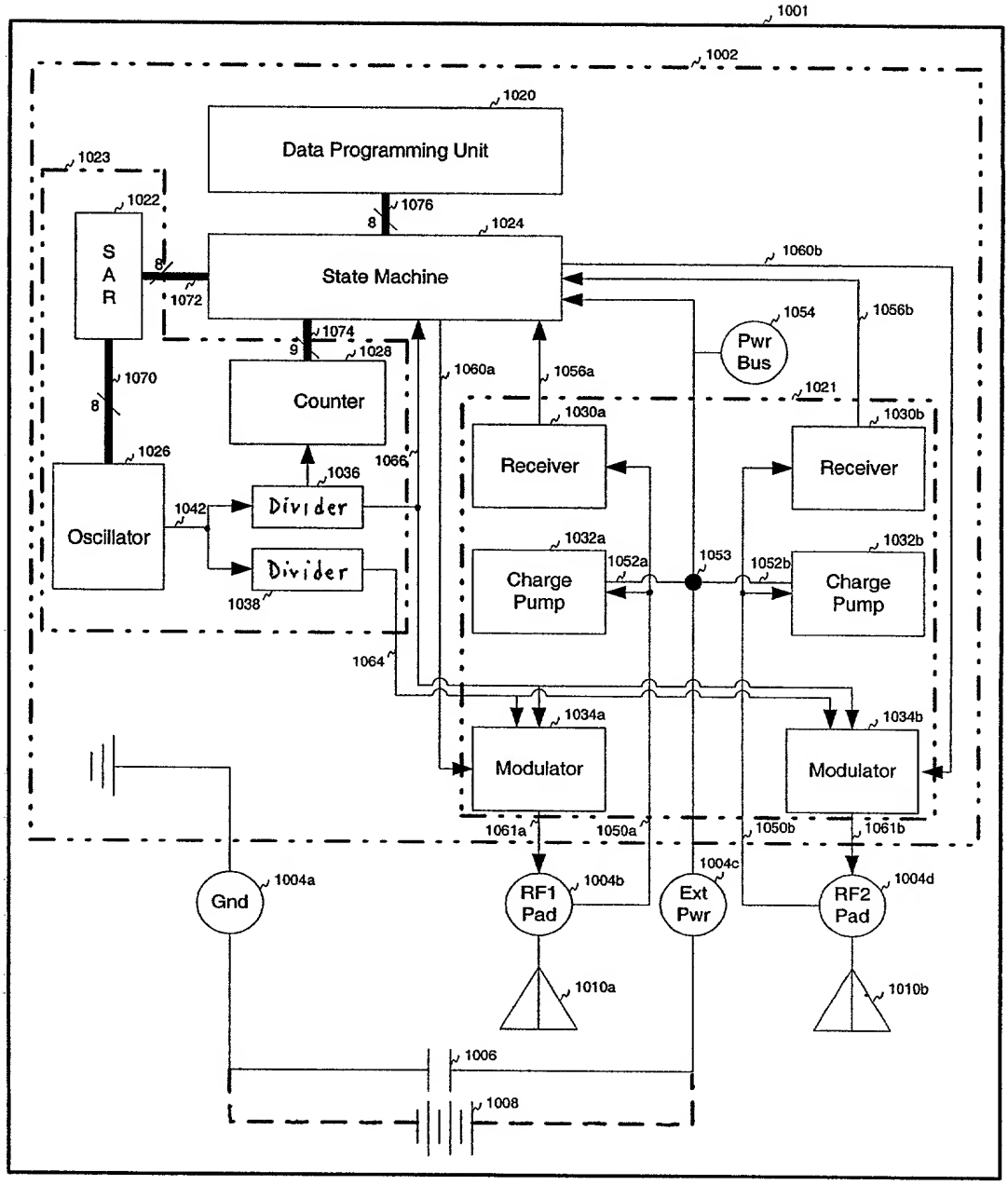

FIG. 10

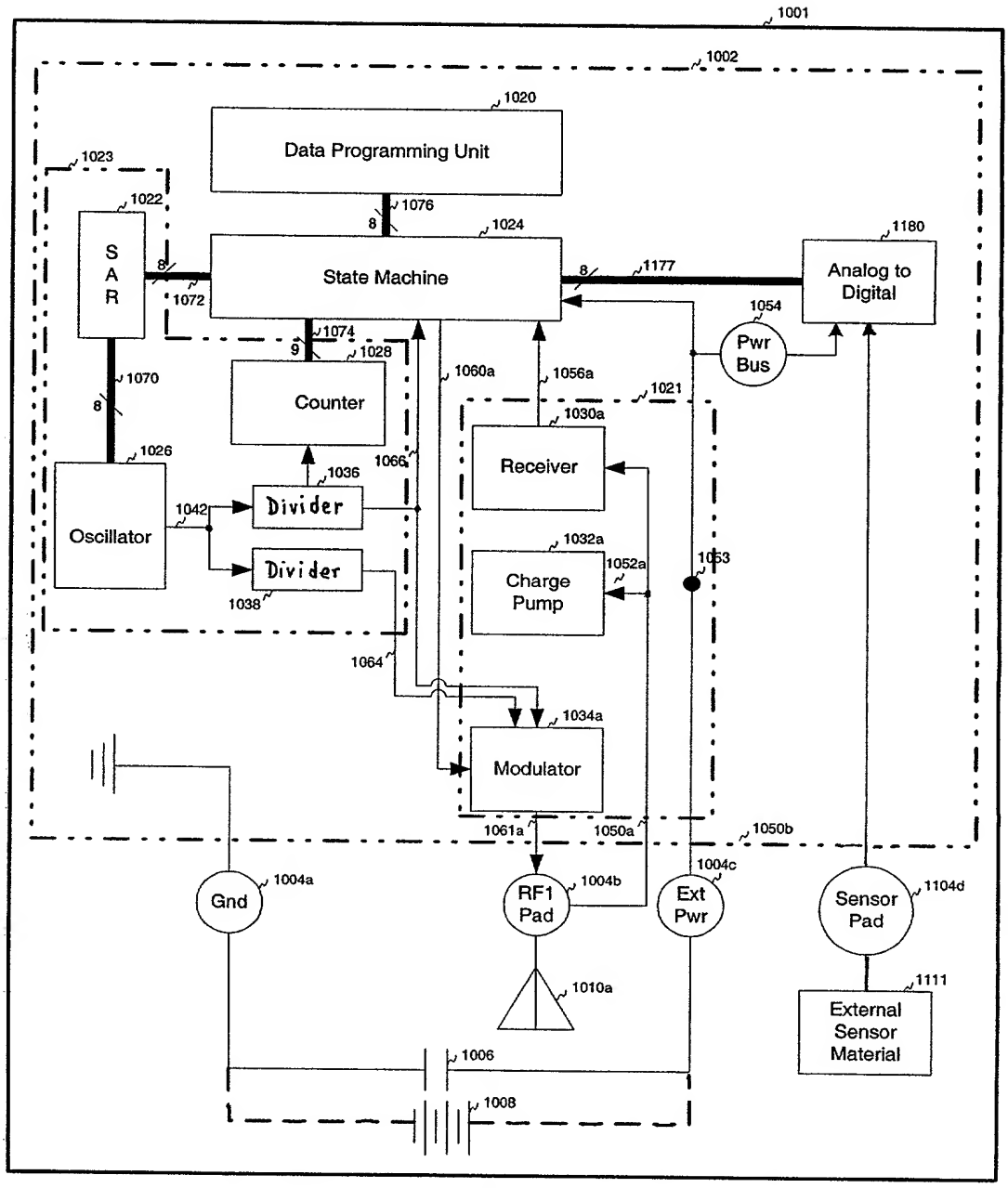

FIG. 11

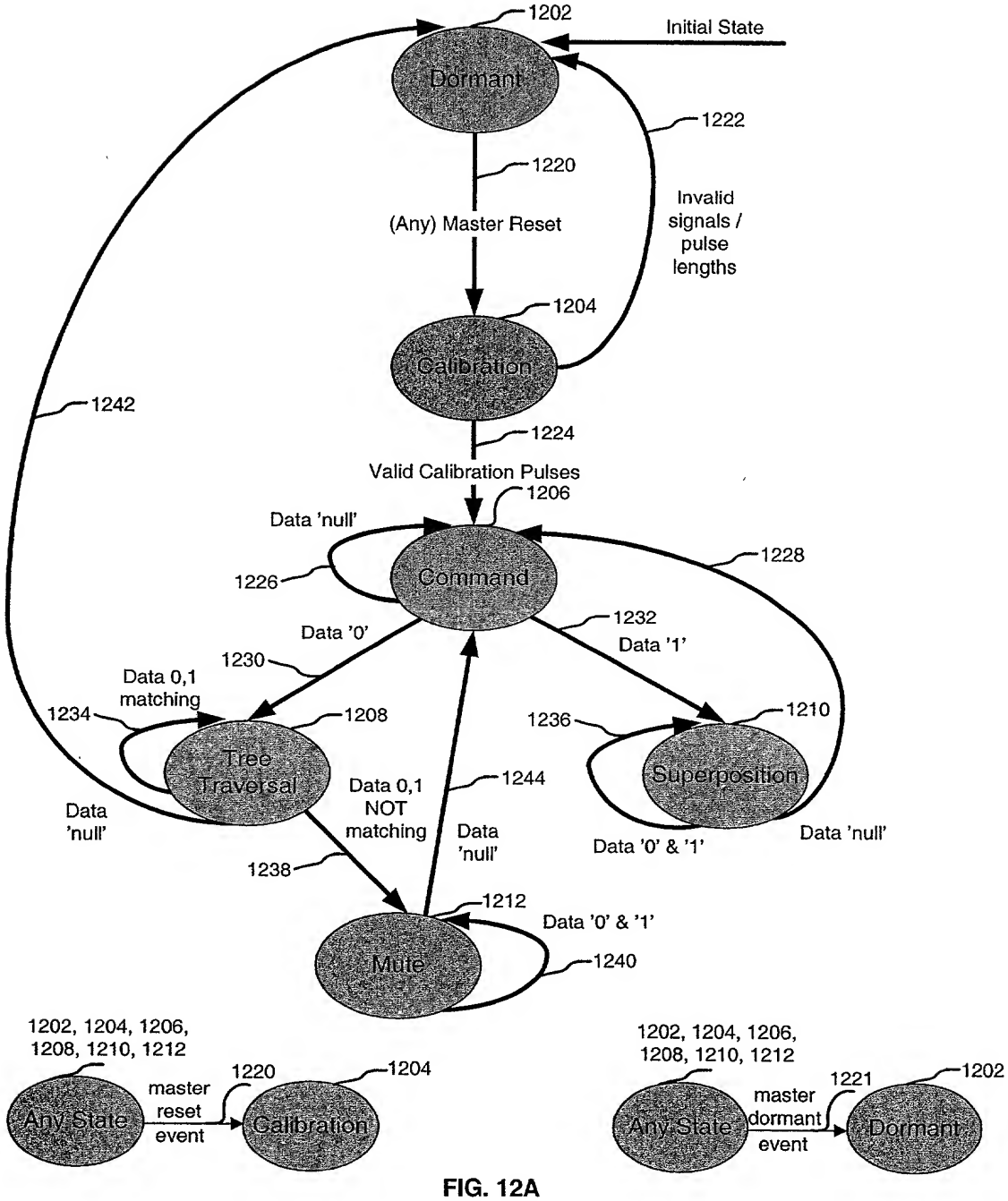

FIG. 12A

0201-20b vsd/8

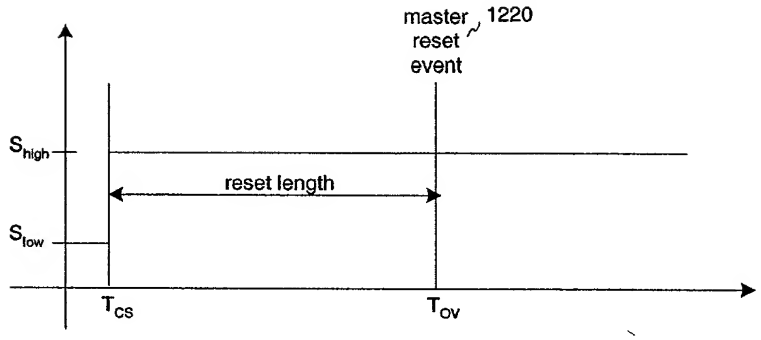

FIG. 12B

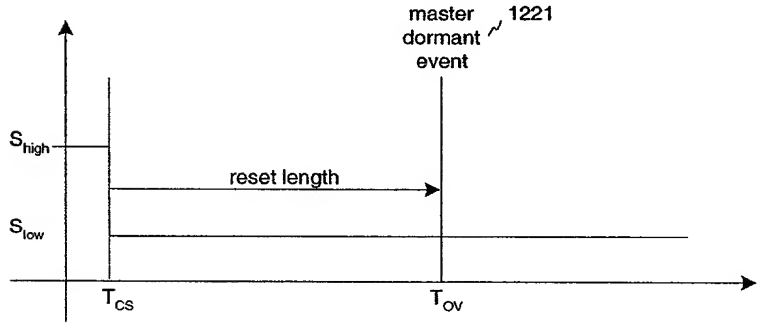

FIG. 12C

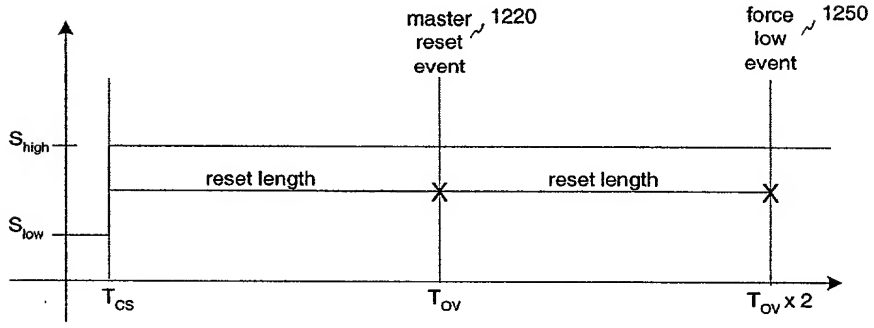

FIG. 12D

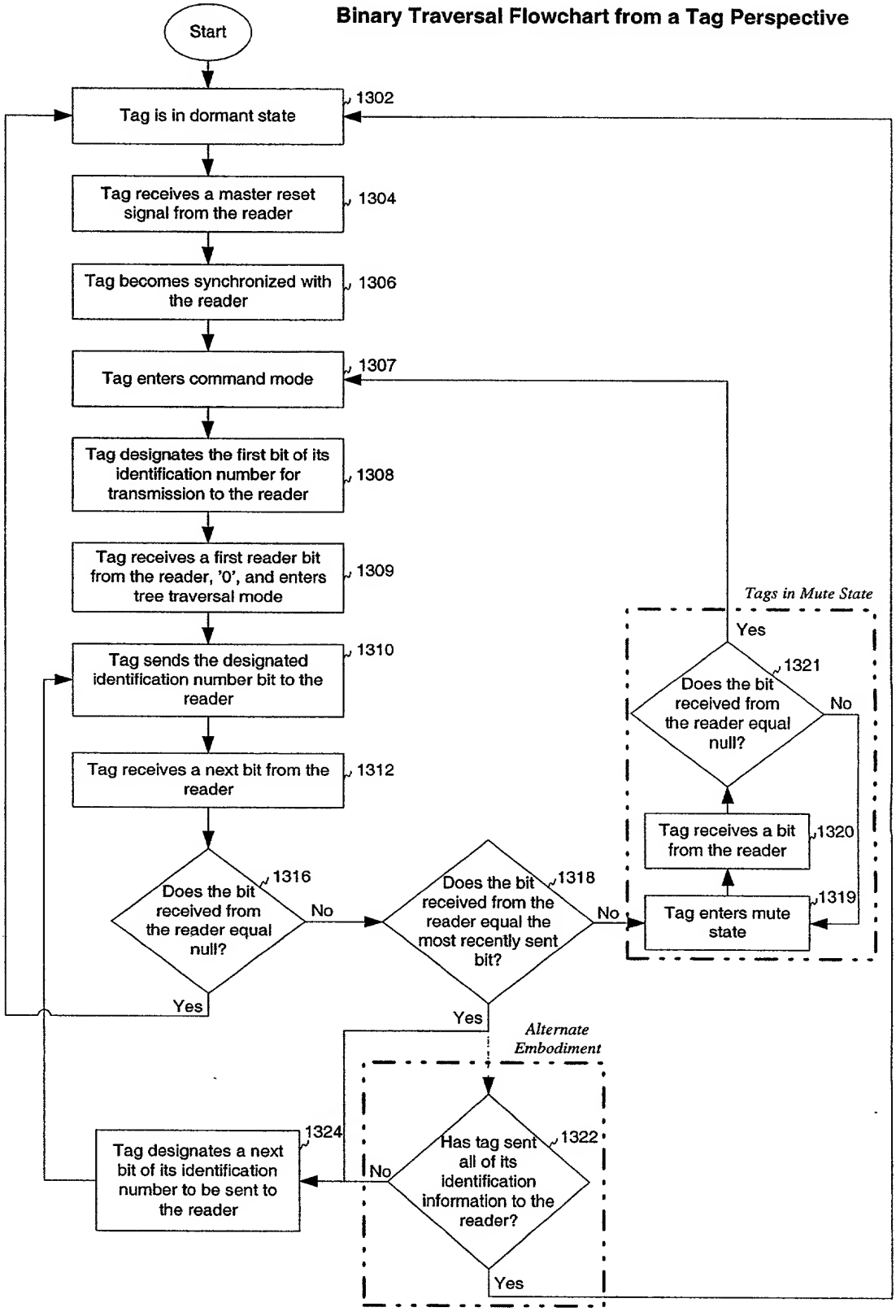

FIG.13

0201-20b.vsd/10

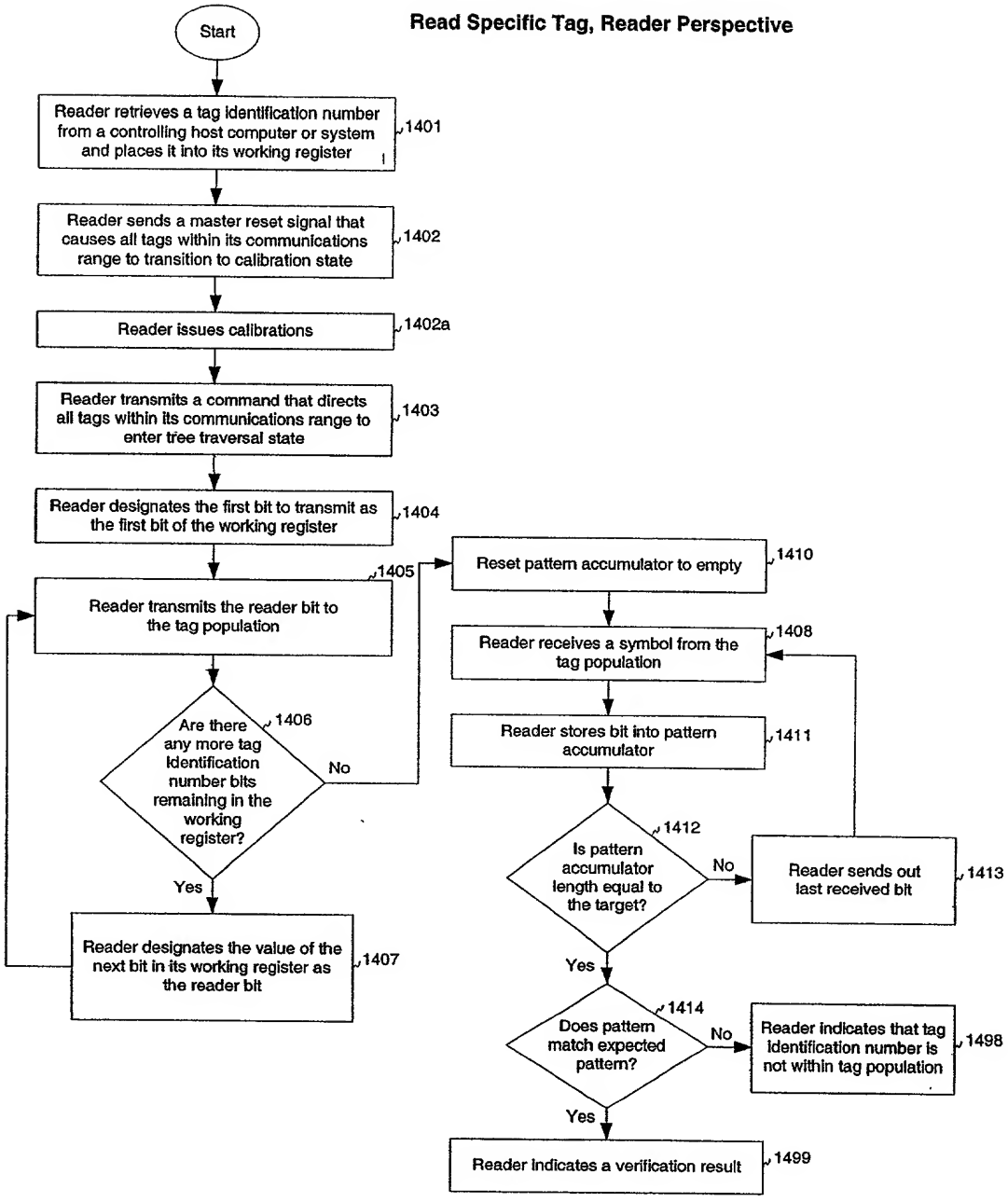

FIG. 14A

0201-20b.vsd/11

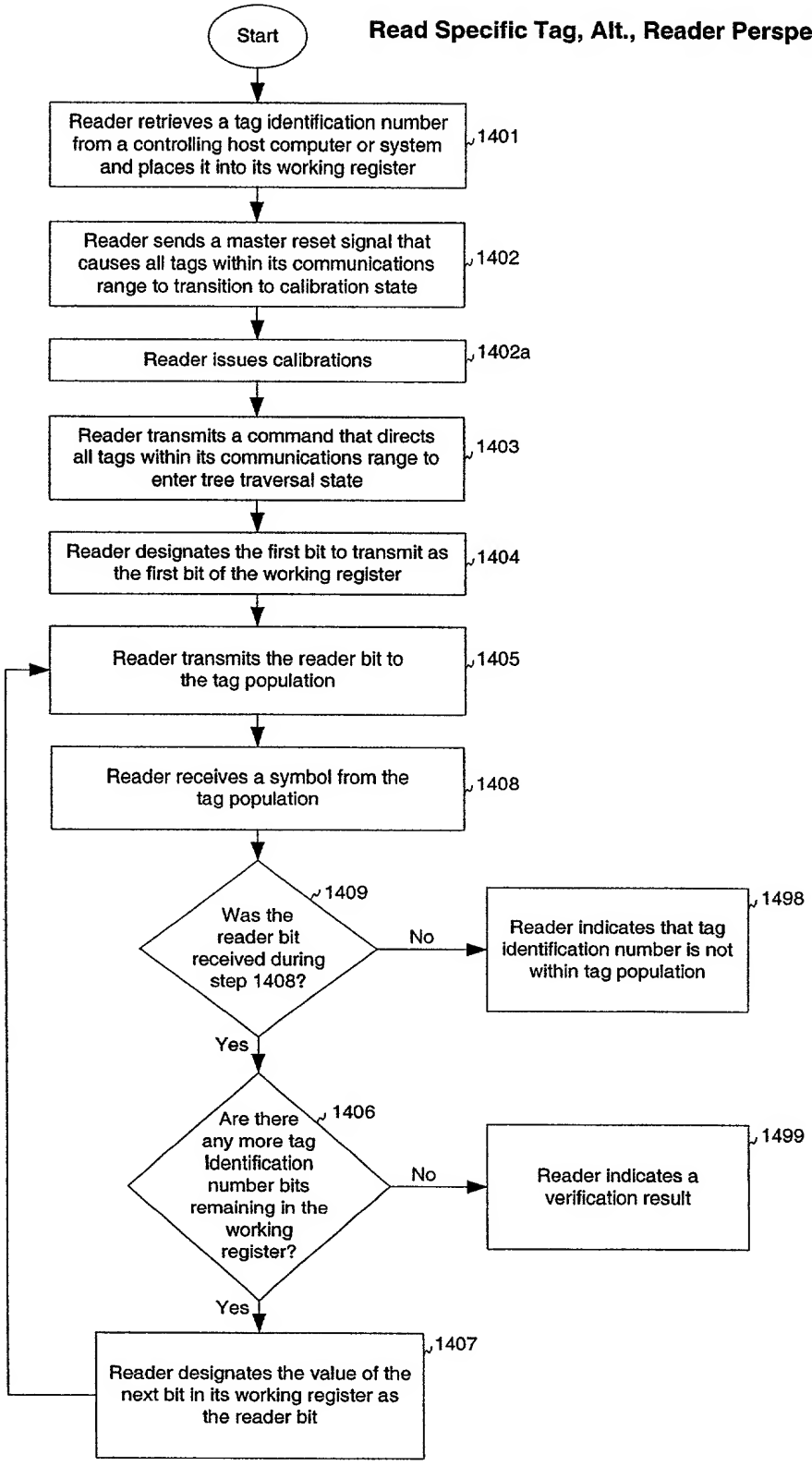

FIG. 14B

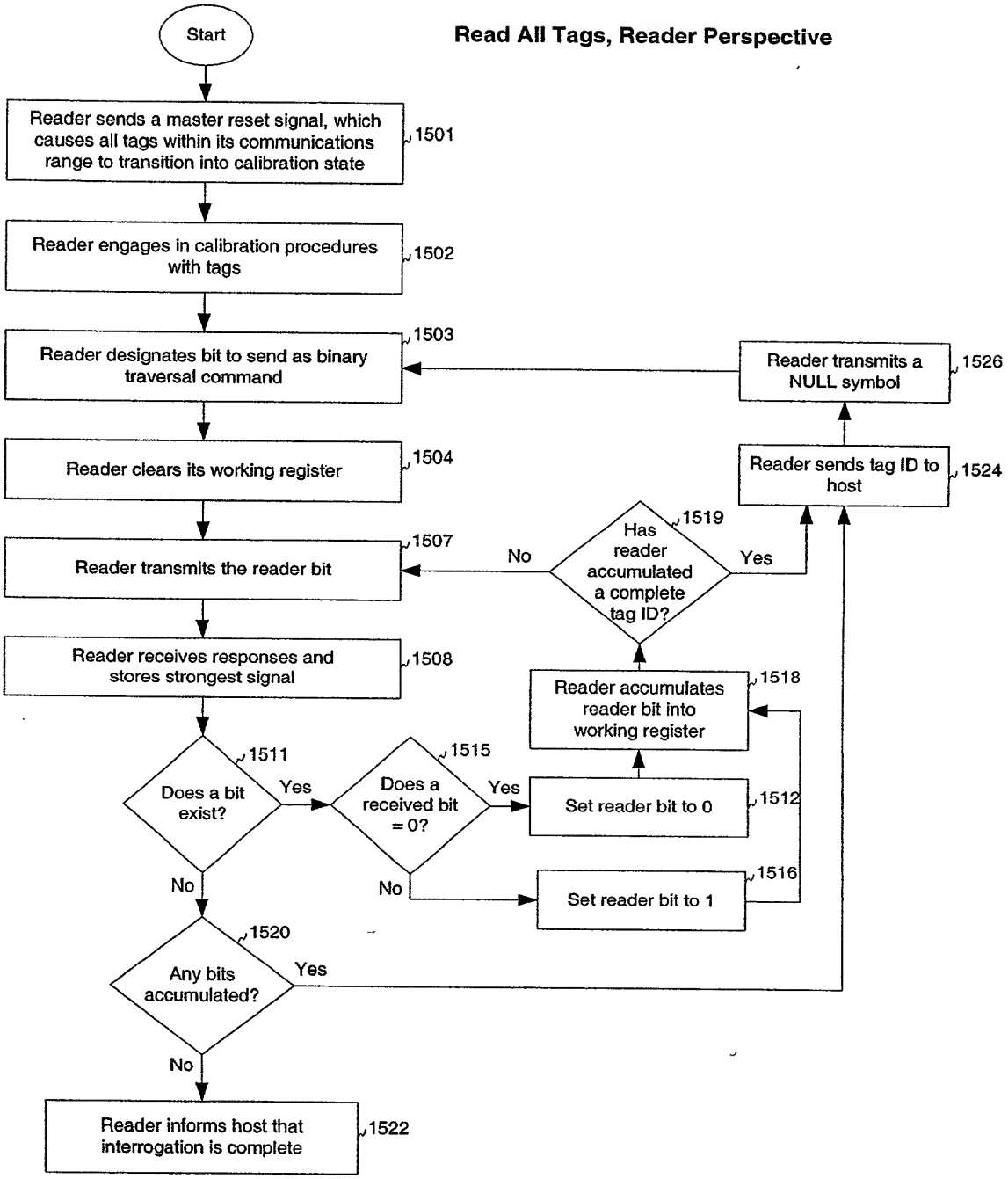

FIG. 15A

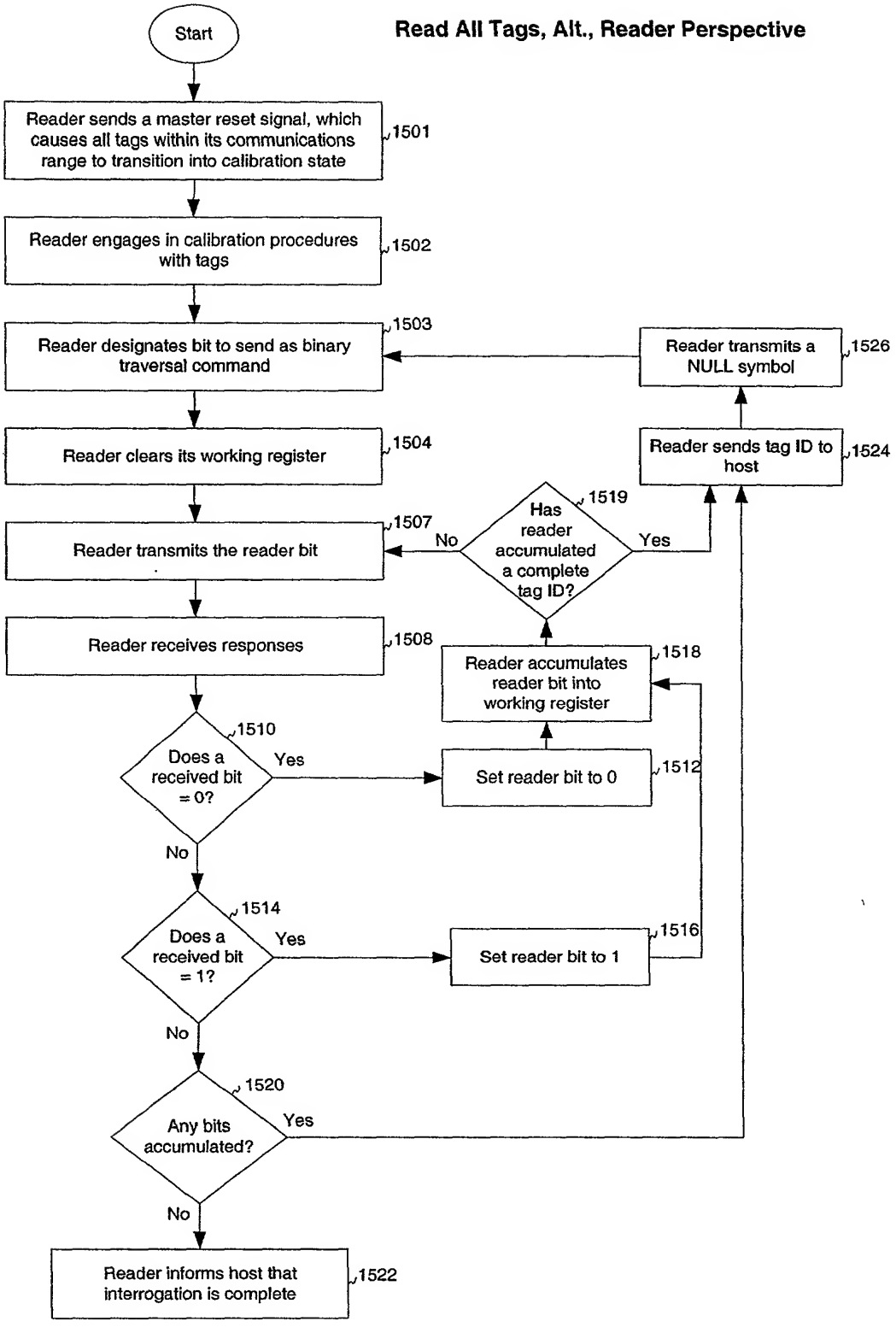

FIG. 15B

Binary Traversal Paths and Tree for a 3-bit Tag Population

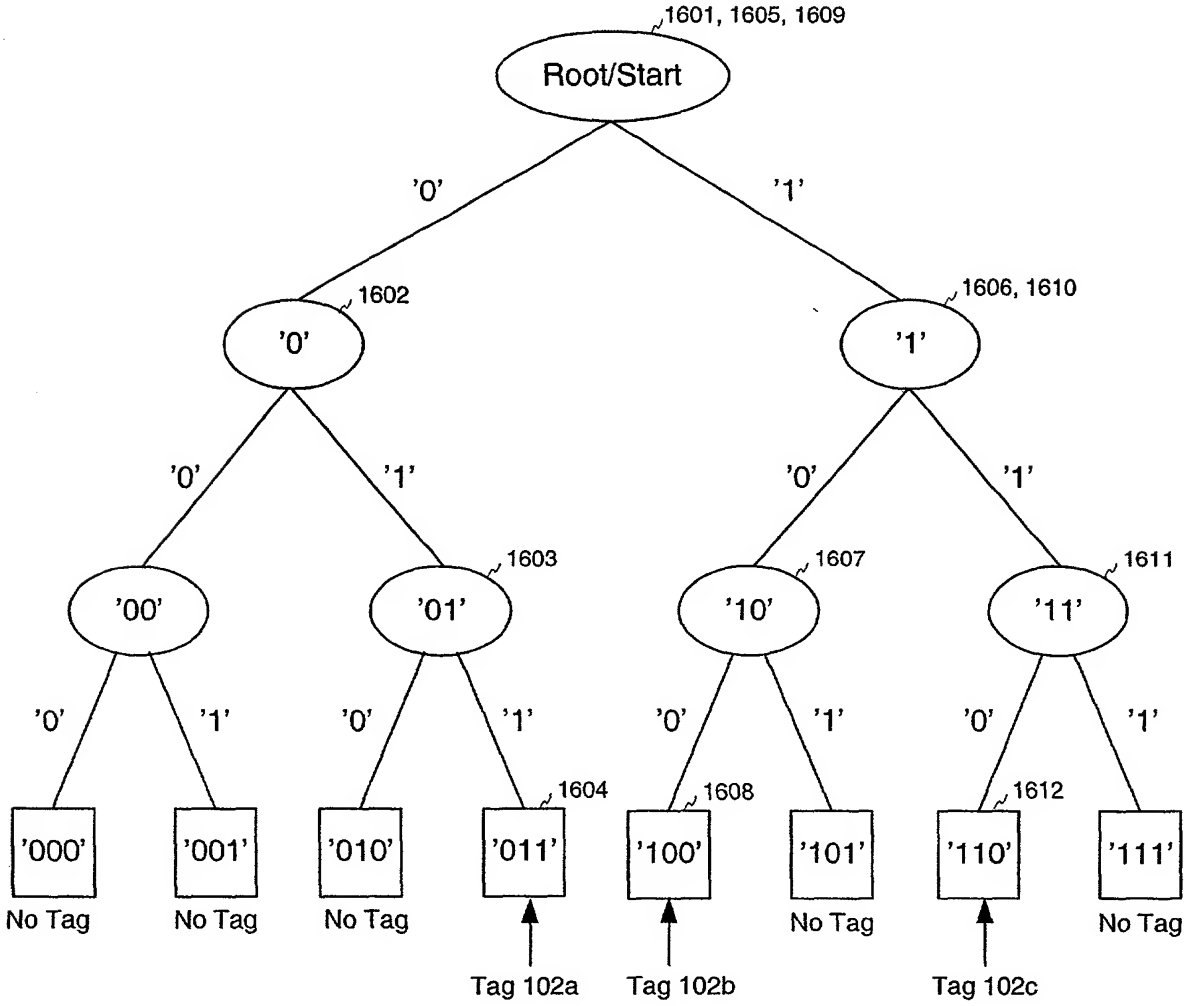

FIG. 16

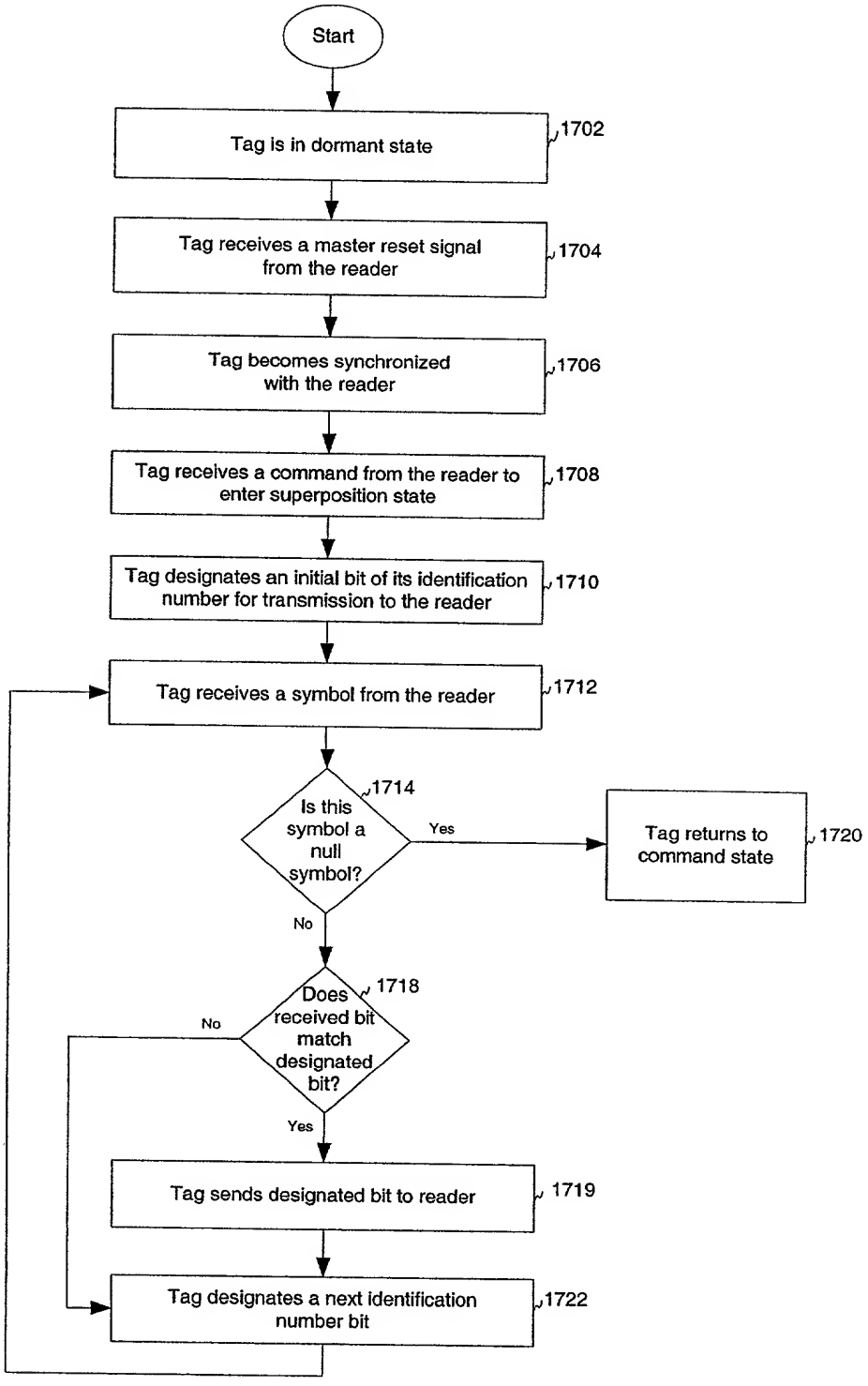

FIG. 17A

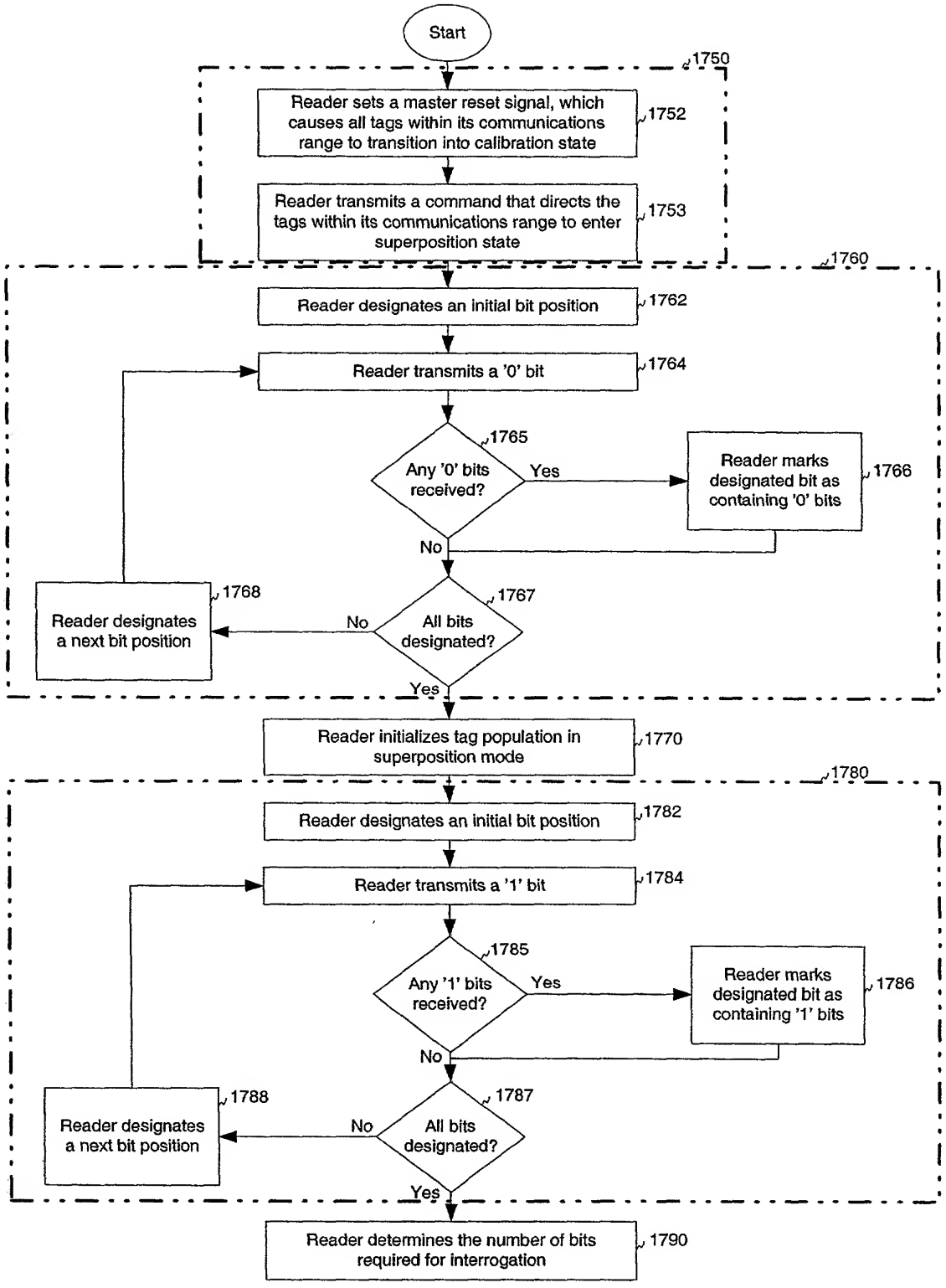
Start
1750
Reader sets a master reset signal, which causes all tags within its communications range to transition into calibration state
1752
Reader transmits a command that directs the tags within its communications range to enter superposition state
1753
1760
Reader designates an initial bit position
1762
Reader transmits a '0' bit
1764
Any '0' bits received?
1765
Yes
Reader marks designated bit as containing '0' bits
1766
No
All bits designated?
1767
No
Reader designates a next bit position
1768
Yes
Reader initializes tag population in superposition mode
1770
1780
Reader designates an initial bit position
1782
Reader transmits a '1' bit
1784
Any '1' bits received?
1785
Yes
Reader marks designated bit as containing '1' bits
1786
No
All bits designated?
1787
No
Reader designates a next bit position
1788
Yes
Reader determines the number of bits required for interrogation
1790

FIG. 17B

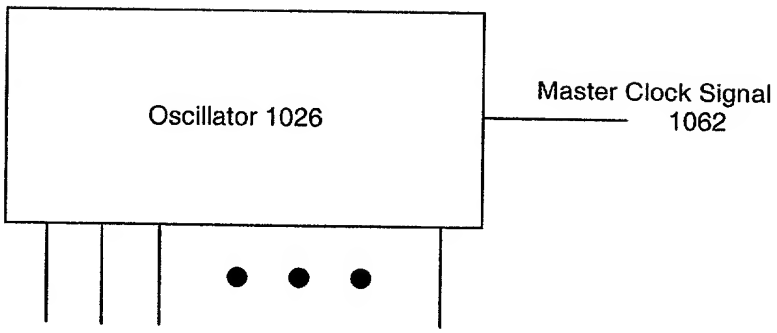
Oscillator 1026
Master Clock Signal
1062
n-bit control word 1070

FIG. 18

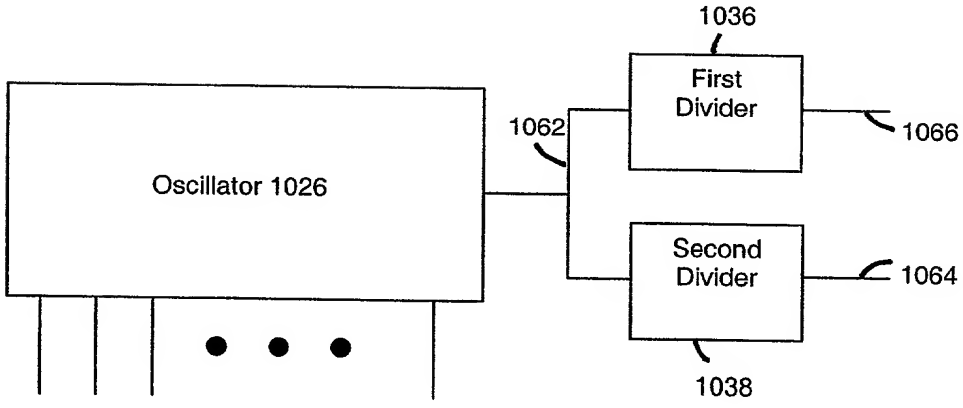
1036
First
Divider
1062
1066
Oscillator 1026
Second
Divider
1064
1038
n-bit control word 1070

FIG. 19

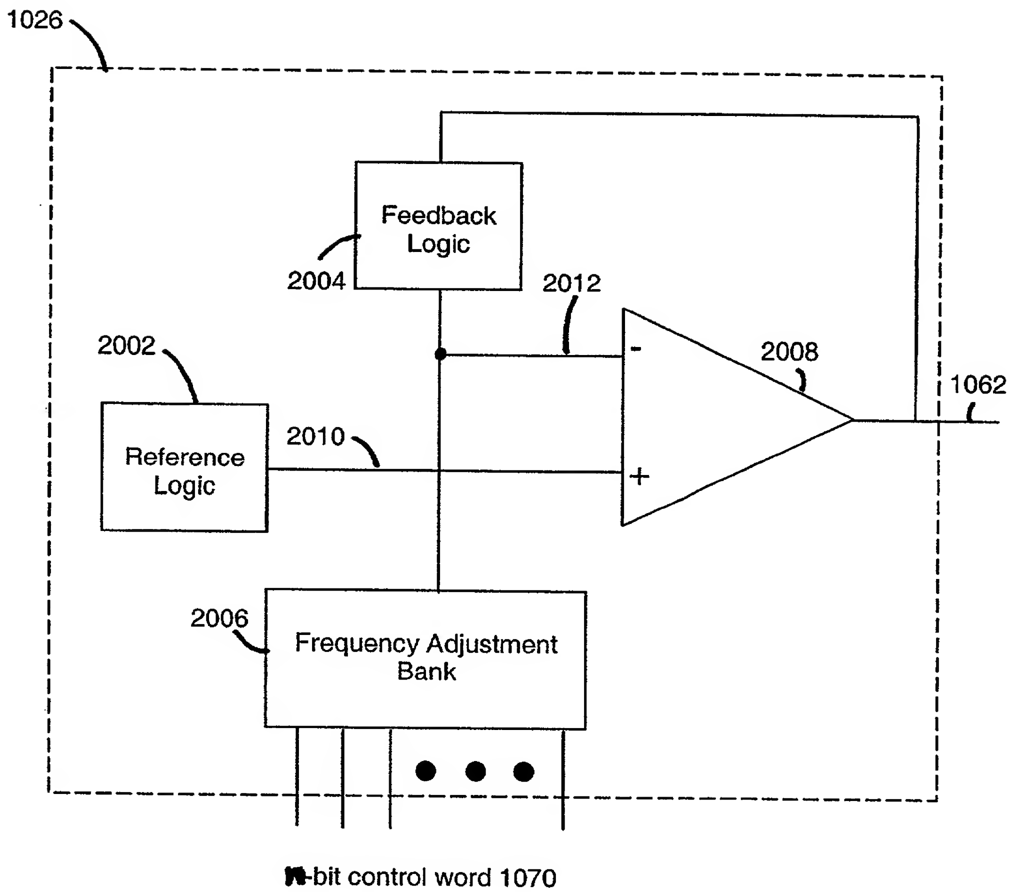
1026
Feedback
Logic
2004
2012
2002
2008
1062
Reference
Logic
2010
-
+
2006
Frequency Adjustment
Bank
N-bit control word 1070

FIG. 20

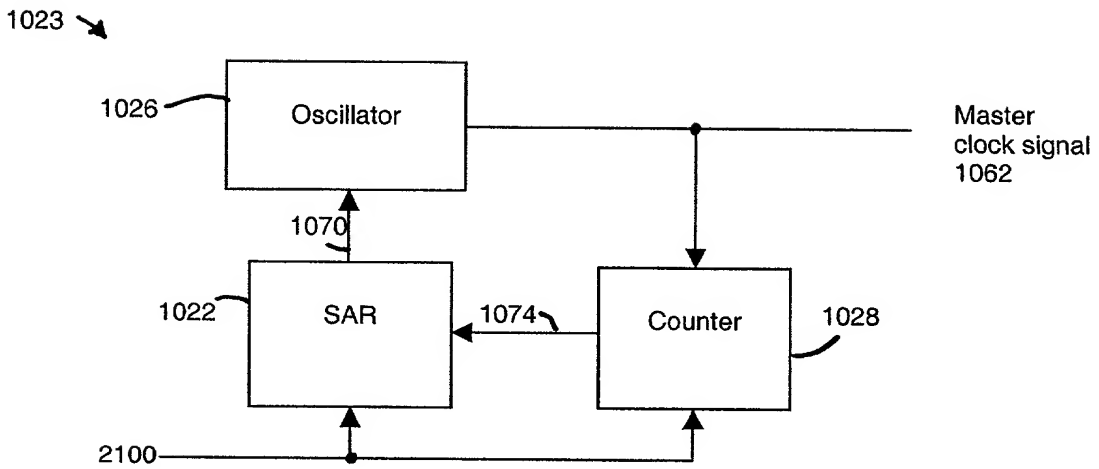

FIG. 21A

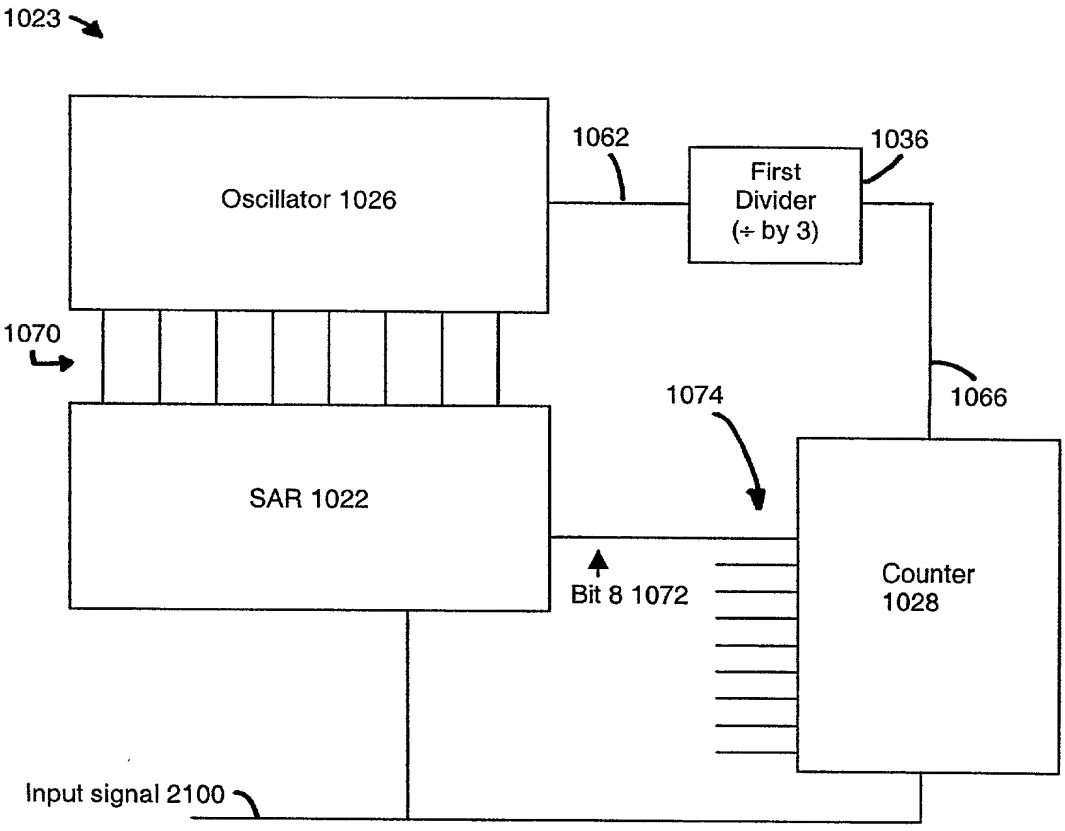

FIG. 21B

0201-20b.vsd/20

Conceptual implementation of SAR calibration

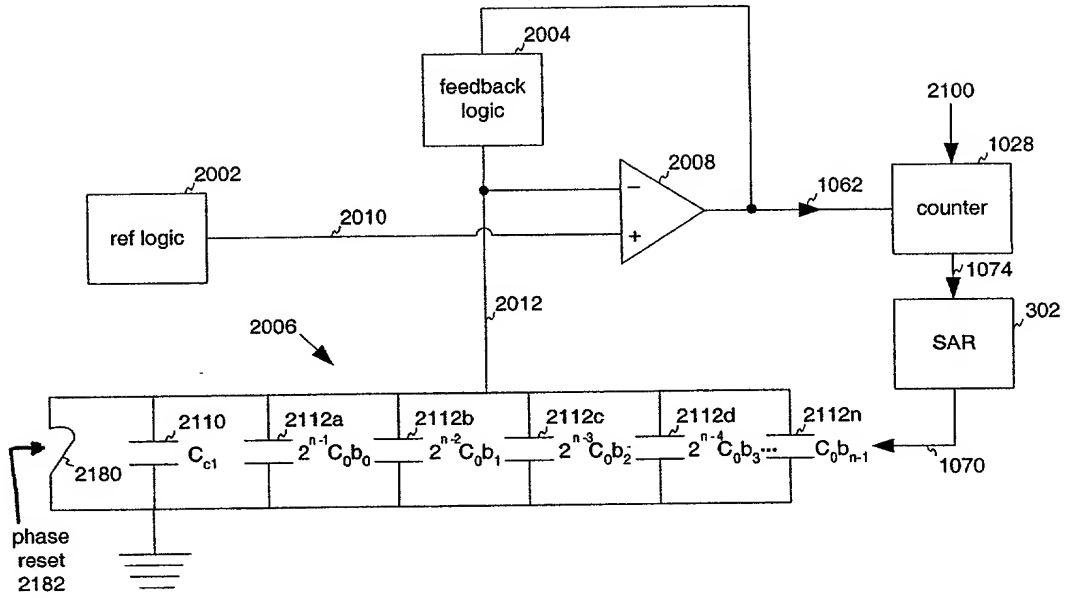

FIG. 21C

Physical implementation of adjustable capacitor bank

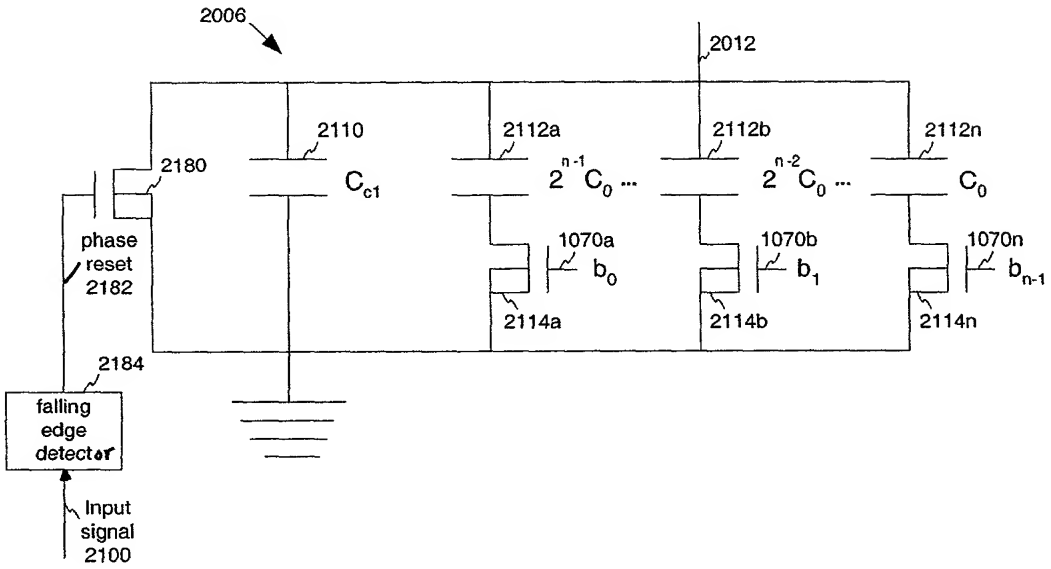

FIG. 21D

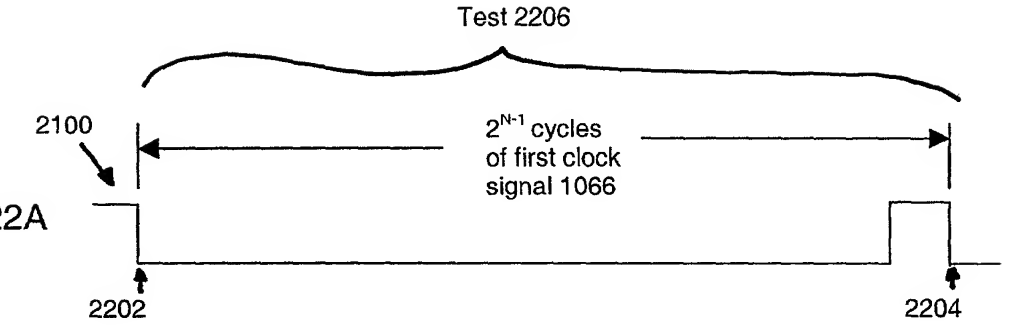

FIG. 22A

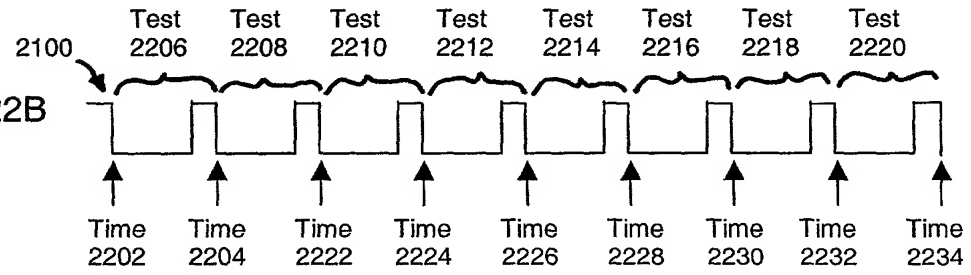

FIG. 22B

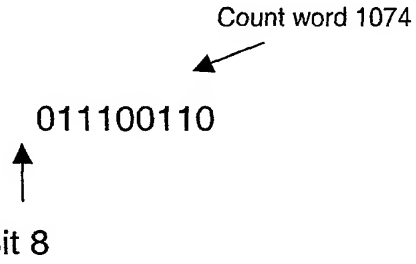

FIG. 23A

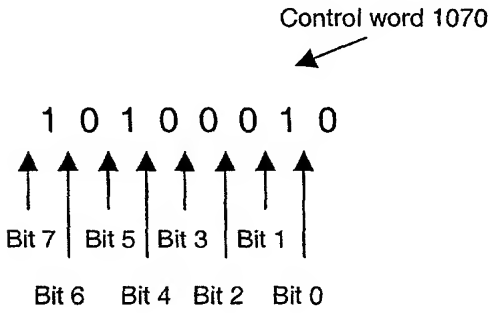

FIG. 23B

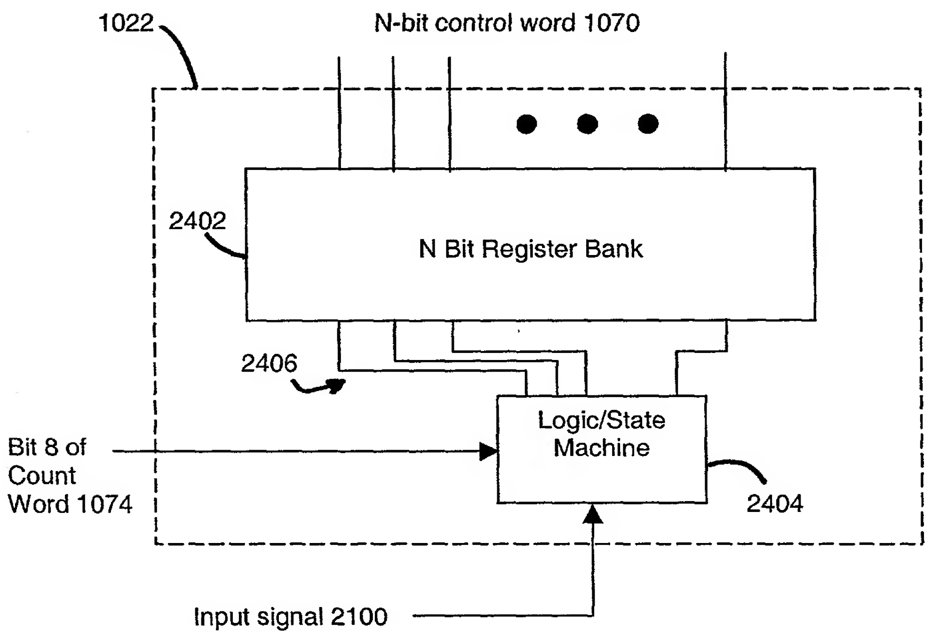
1022
N-bit control word 1070
2402
N Bit Register Bank
2406
Logic/State
Machine
Bit 8 of
Count
Word 1074
2404
Input signal 2100

FIG. 24

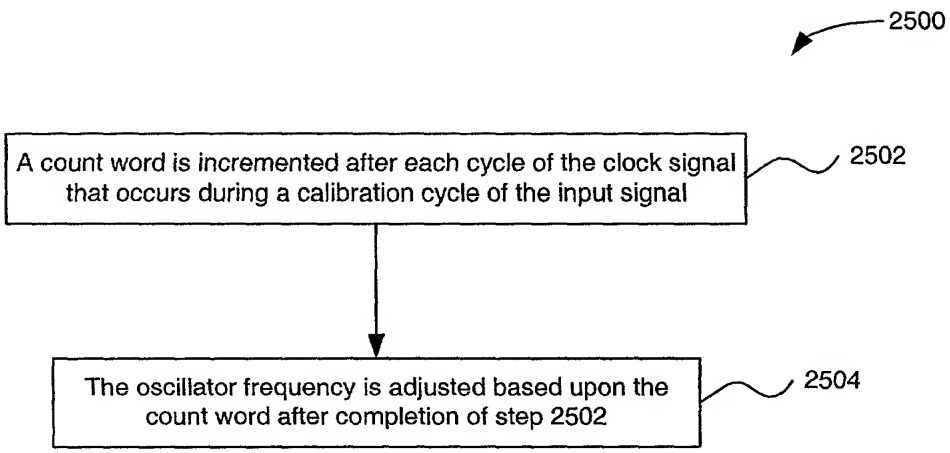

FIG. 25A

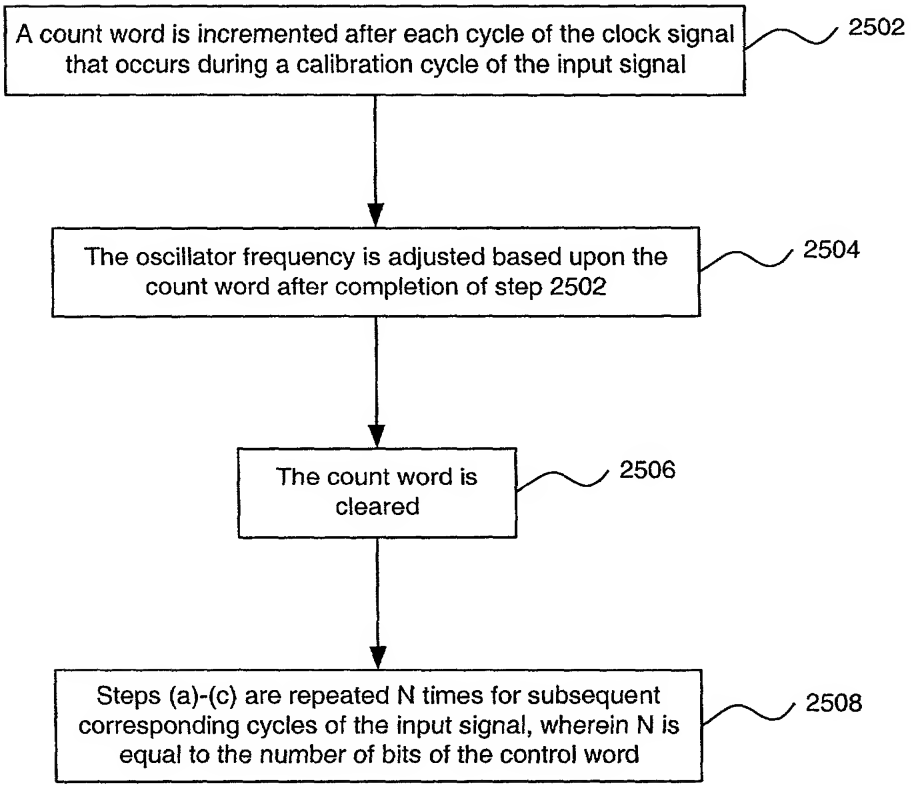

FIG. 25B

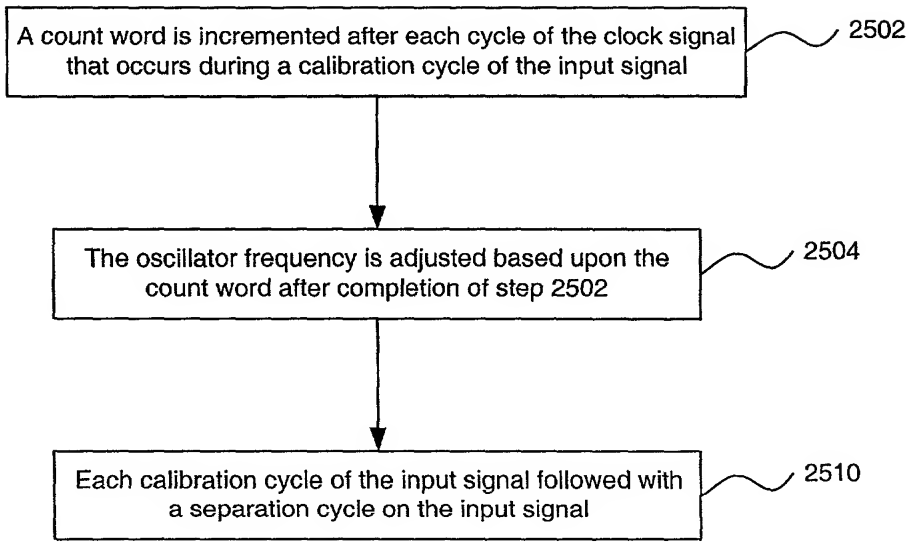

FIG. 25C

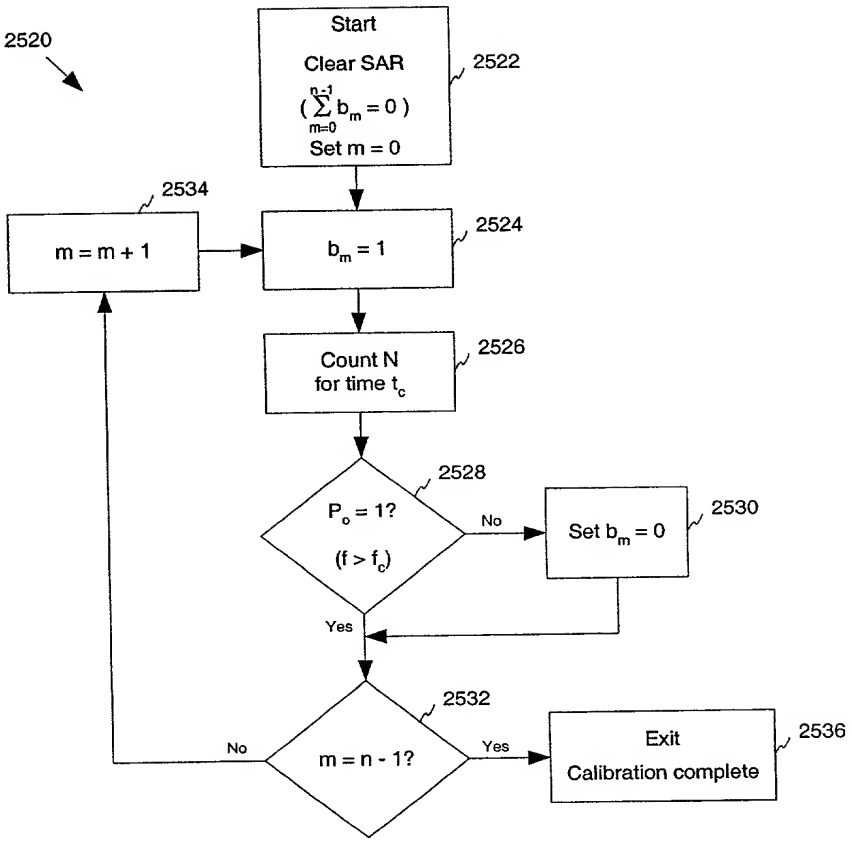

FIG. 25D

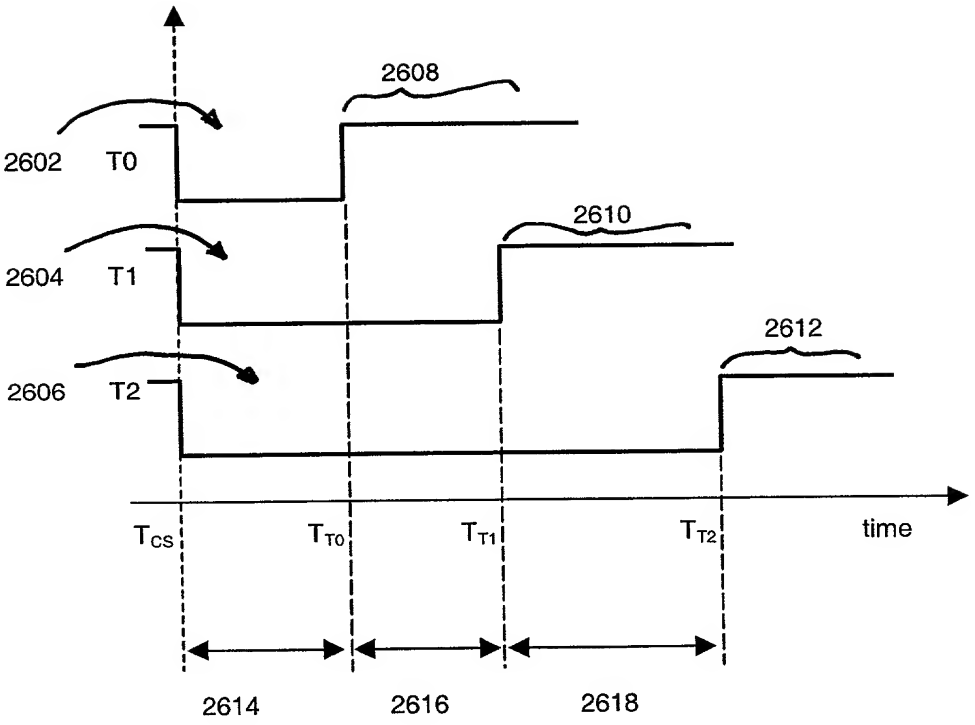

FIG. 26A

Data Symbol Timing Chart

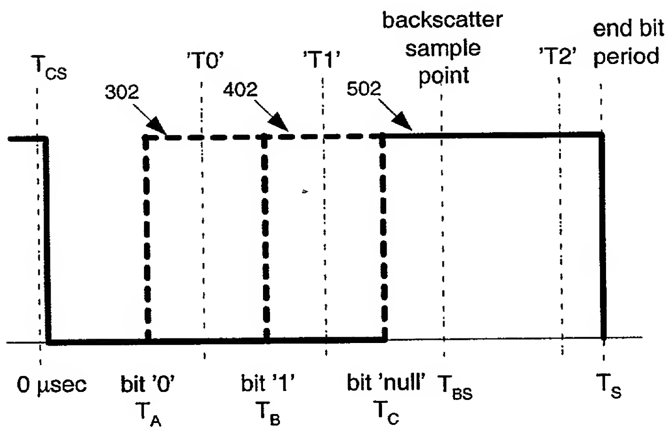

FIG. 26B

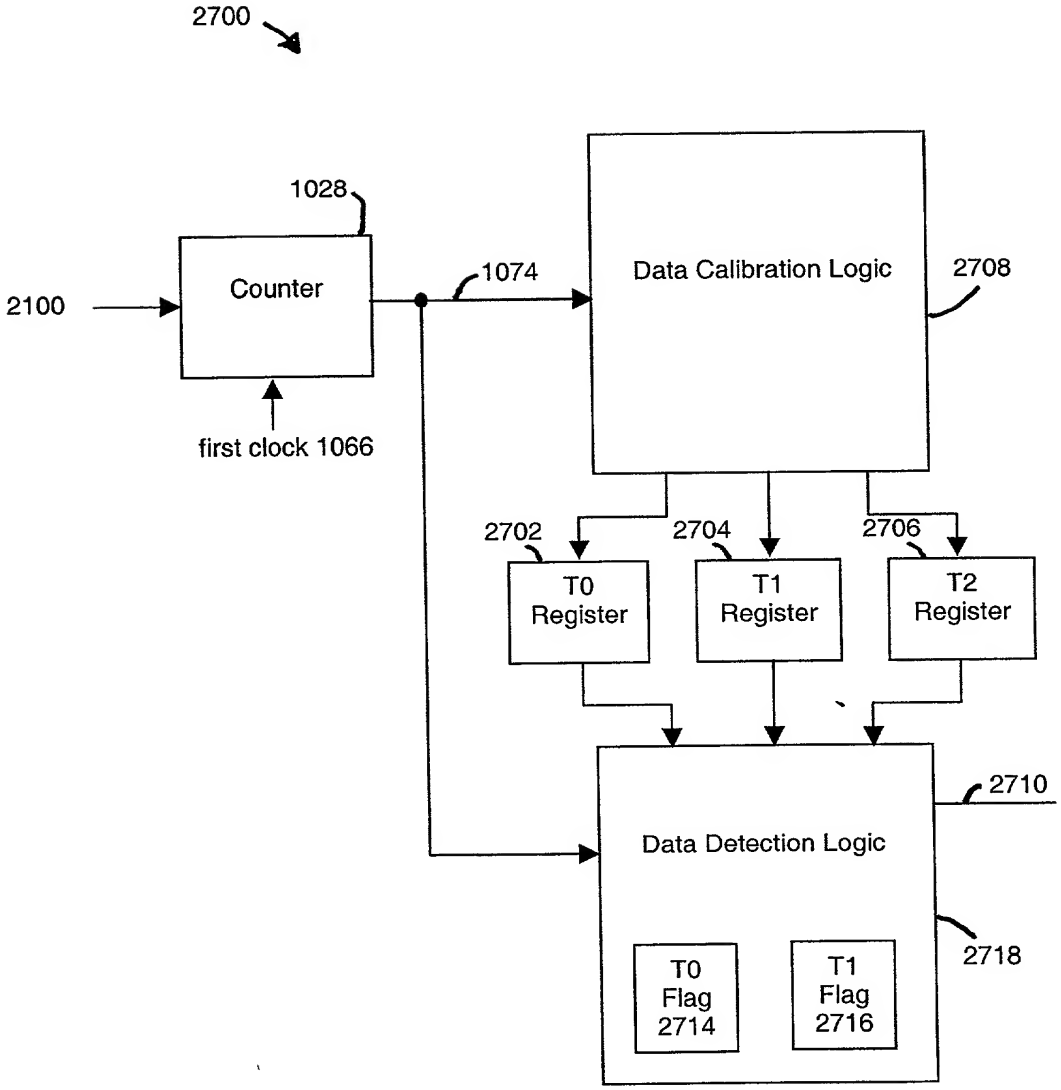

FIG. 27

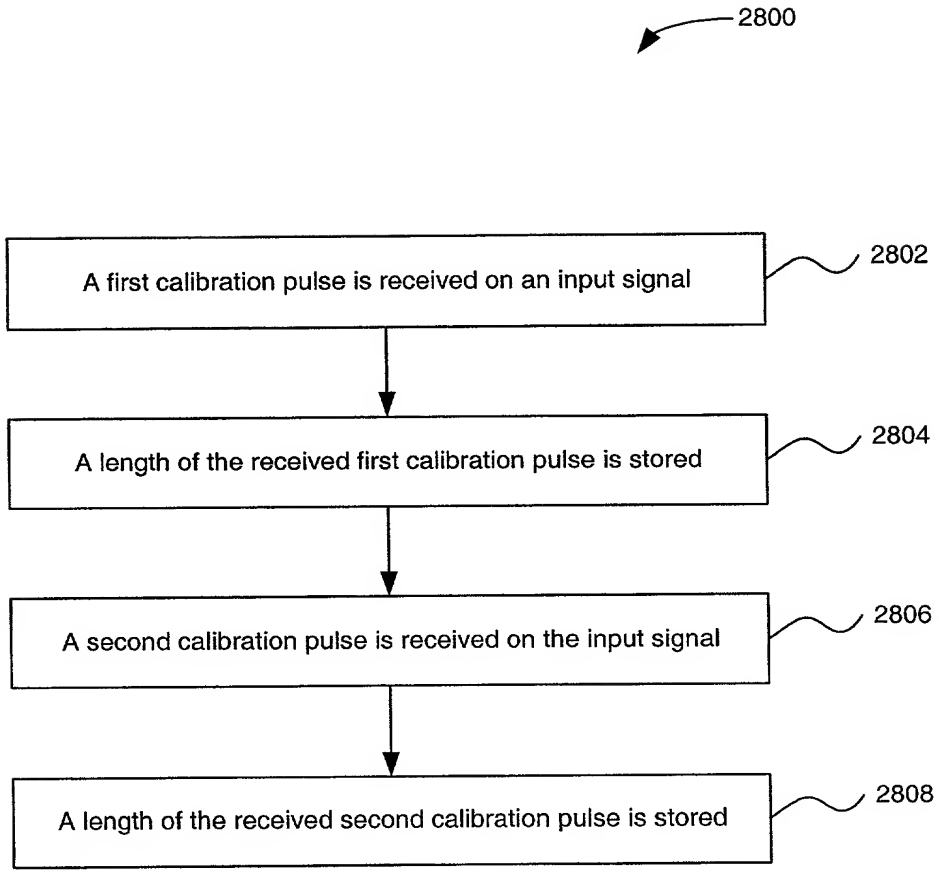
2800
A first calibration pulse is received on an input signal
2802
A length of the received first calibration pulse is stored
2804
A second calibration pulse is received on the input signal
2806
A length of the received second calibration pulse is stored
2808

FIG. 28A

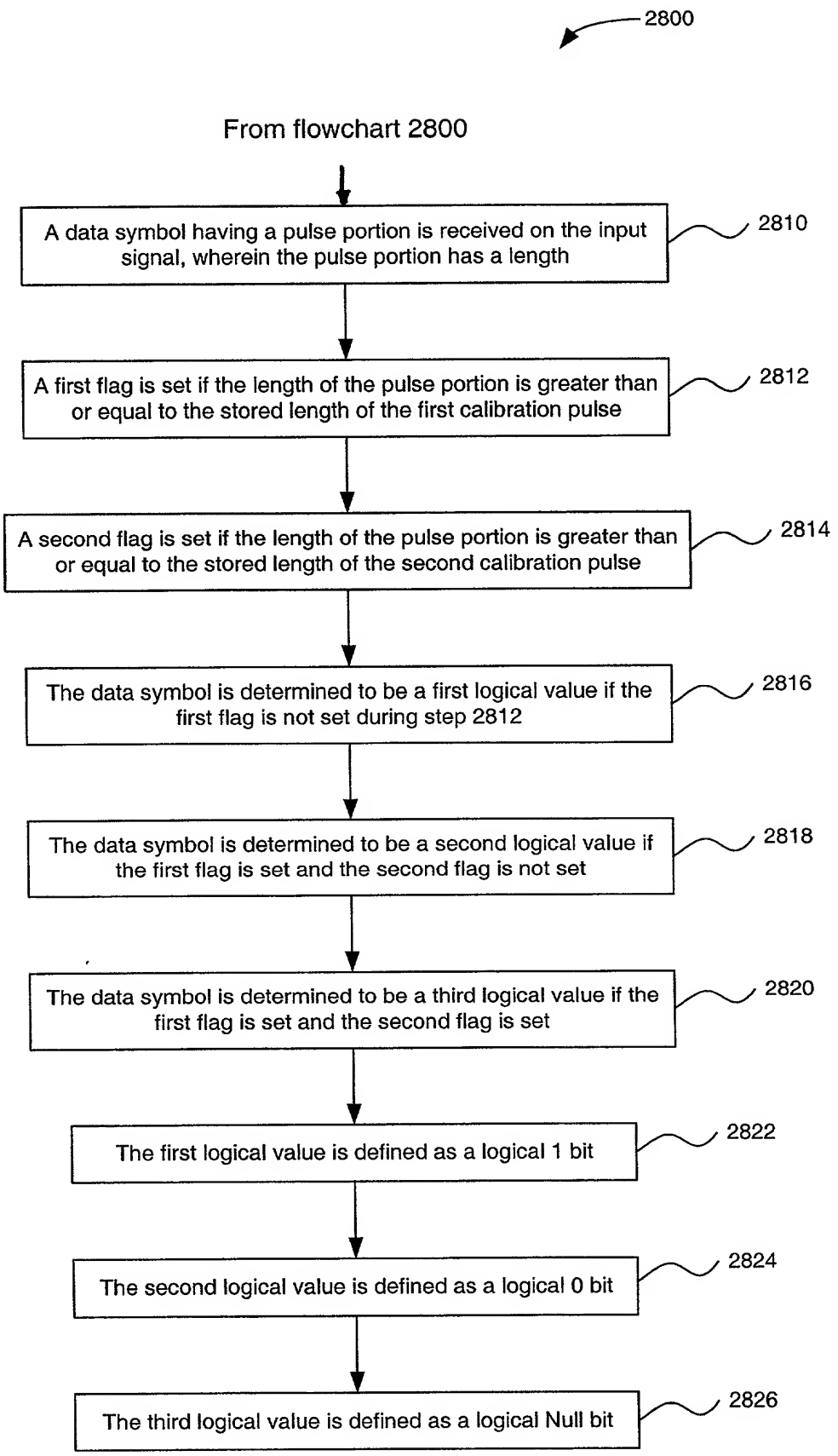

FIG. 28B

0201-20b.vsd/32

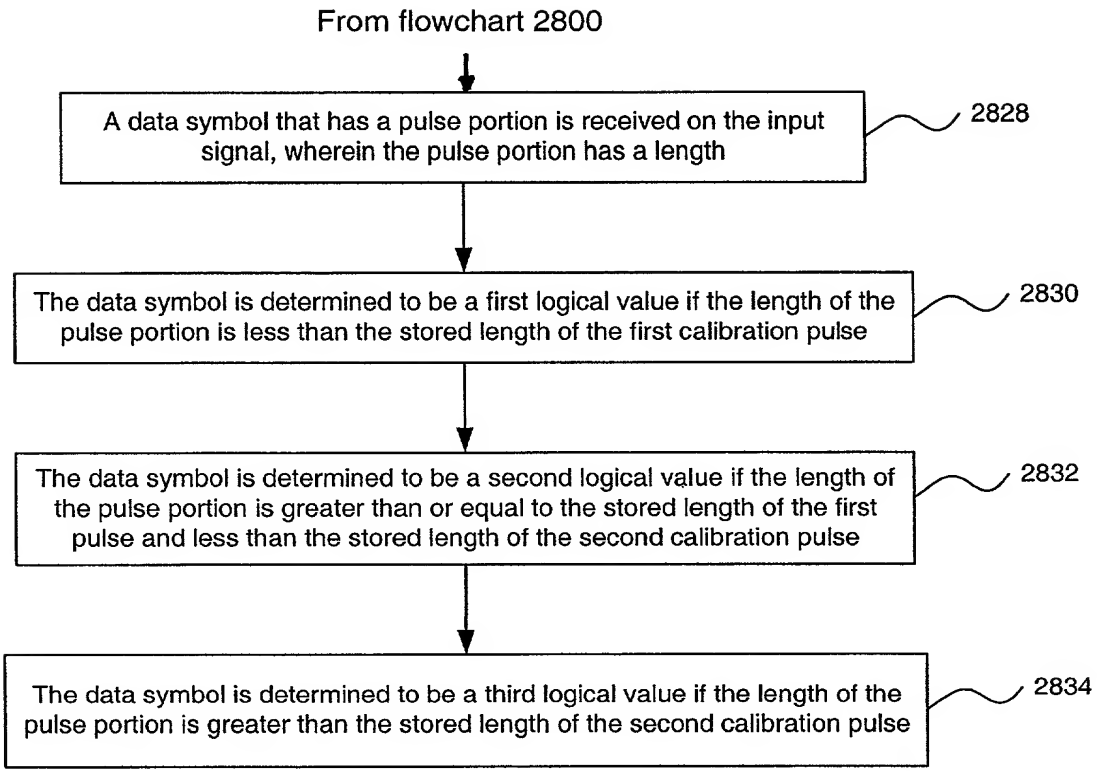

FIG. 28C

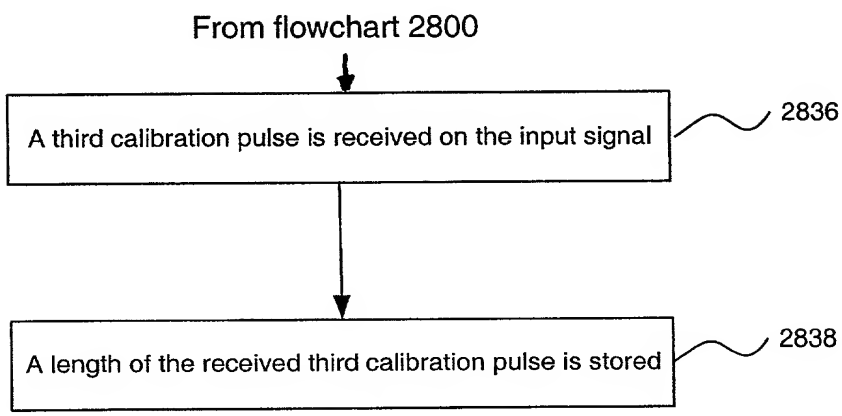
From flowchart 2800
A third calibration pulse is received on the input signal
2836
A length of the received third calibration pulse is stored
2838

FIG. 28D

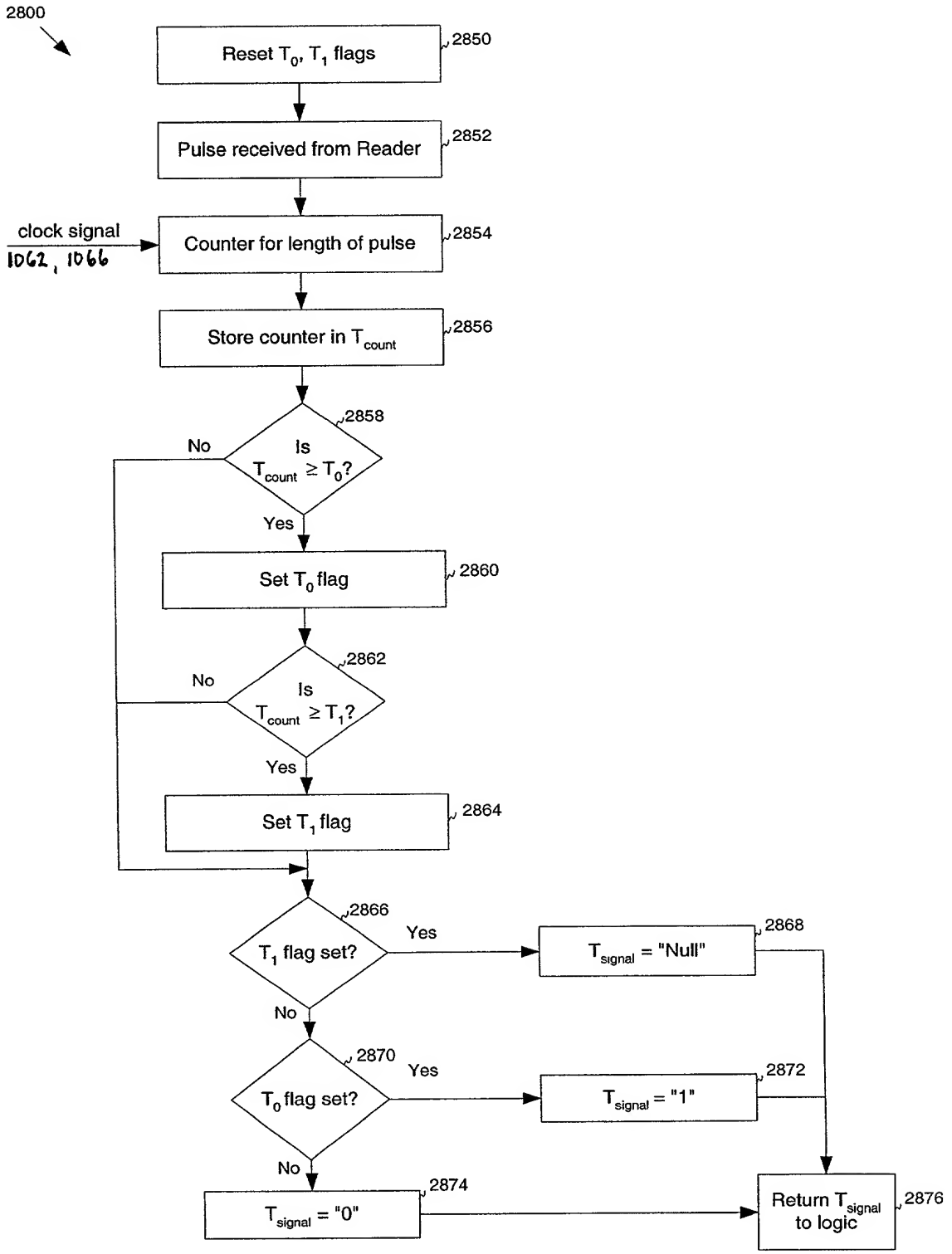
2800
Reset T_0, T_1 flags
2850
Pulse received from Reader
2852
clock signal
1062, 1066
Counter for length of pulse
2854
Store counter in T_{count}
2856
2858
Is $T_{count} \geq T_0$?
No
Yes
Set T_0 flag
2860
2862
Is $T_{count} \geq T_1$?
No
Yes
Set T_1 flag
2864
2866
T_1 flag set?
Yes
T_{signal} = "Null"
2868
No
2870
T_0 flag set?
Yes
T_{signal} = "1"
2872
No
T_{signal} = "0"
2874
Return T_{signal} to logic
2876

FIG. 28E

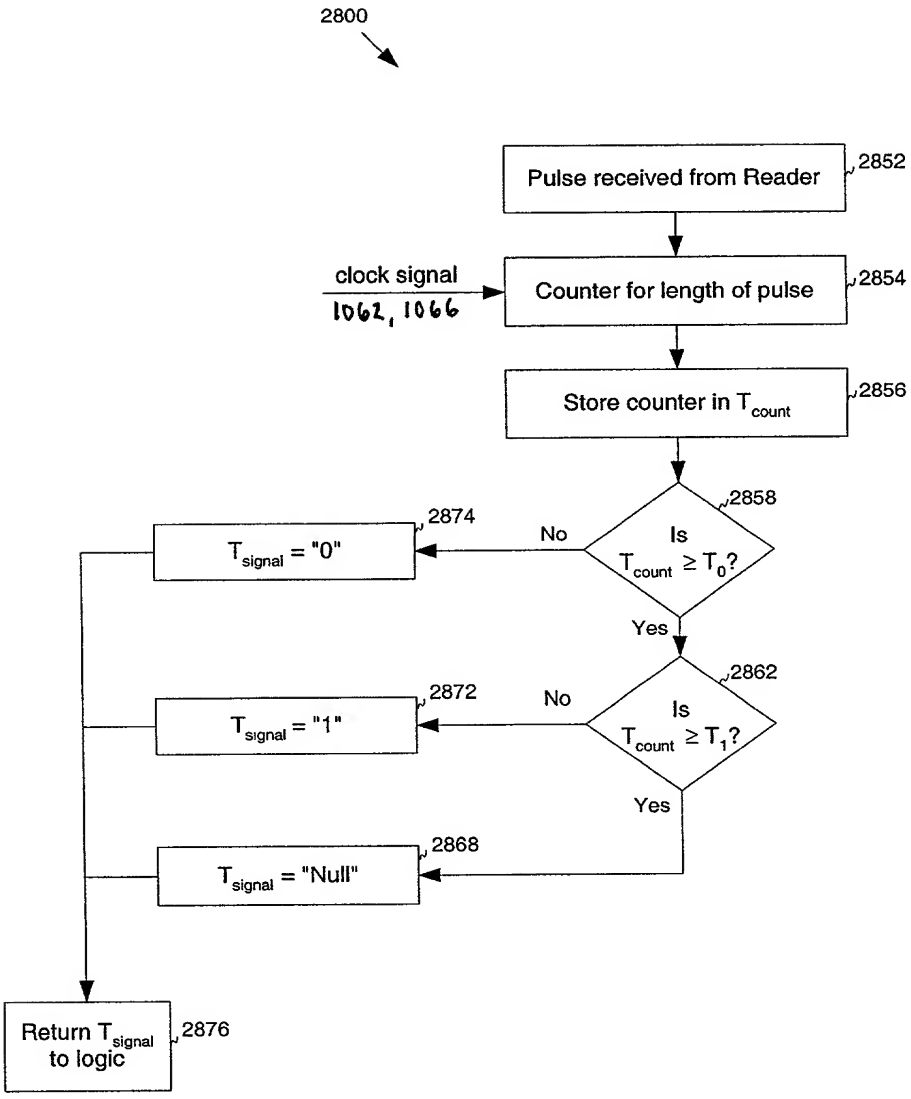
2800
Pulse received from Reader
2852
clock signal
1062, 1066
Counter for length of pulse
2854
Store counter in T_{count}
2856
Is $T_{count} \geq T_0$?
2858
No
T_{signal} = "0"
2874
Yes
Is $T_{count} \geq T_1$?
2862
No
T_{signal} = "1"
2872
Yes
T_{signal} = "Null"
2868
Return T_{signal} to logic
2876

FIG. 28F

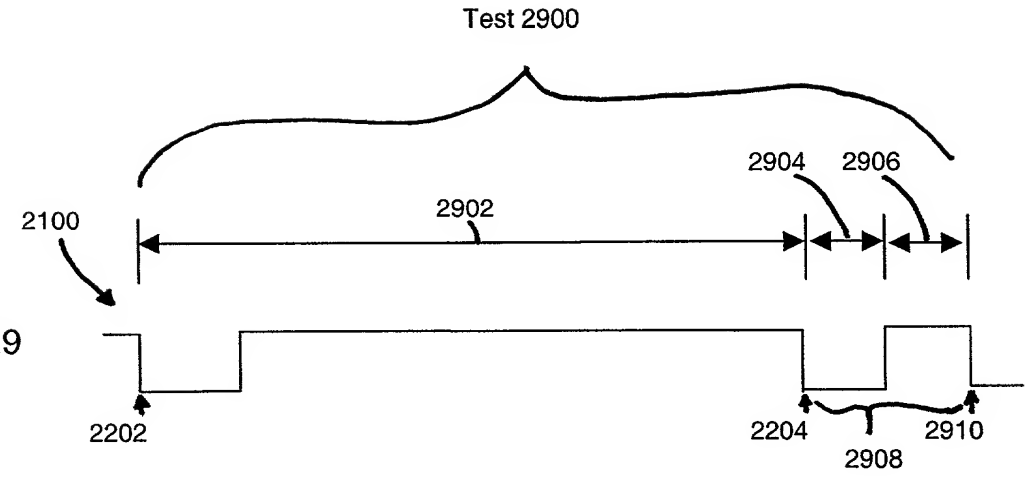

FIG. 29

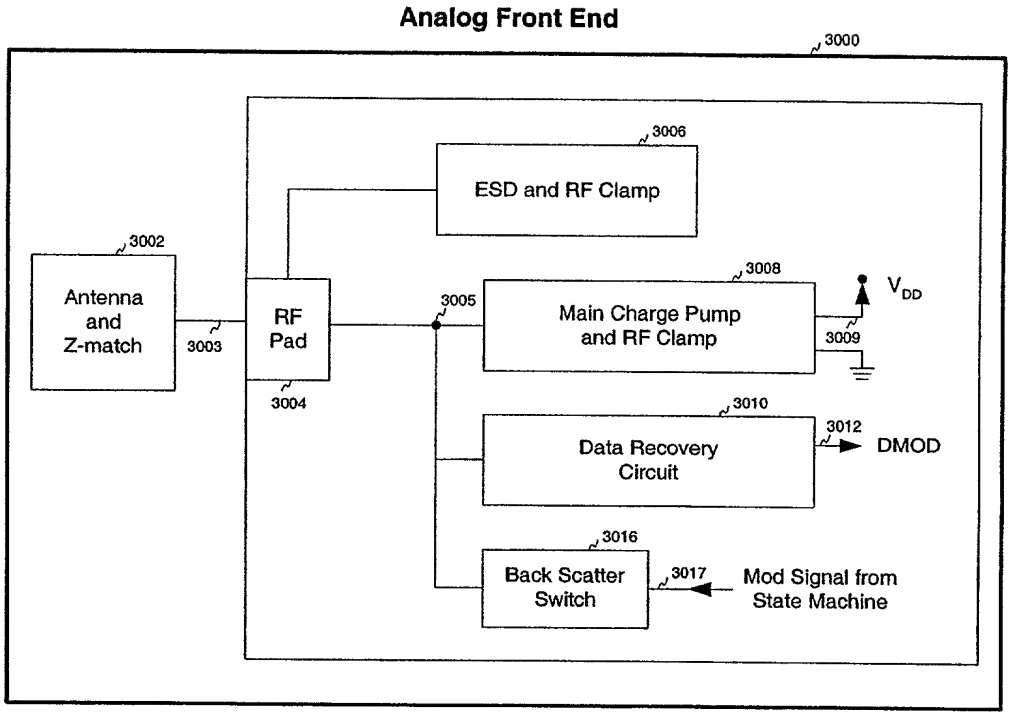

FIG. 30

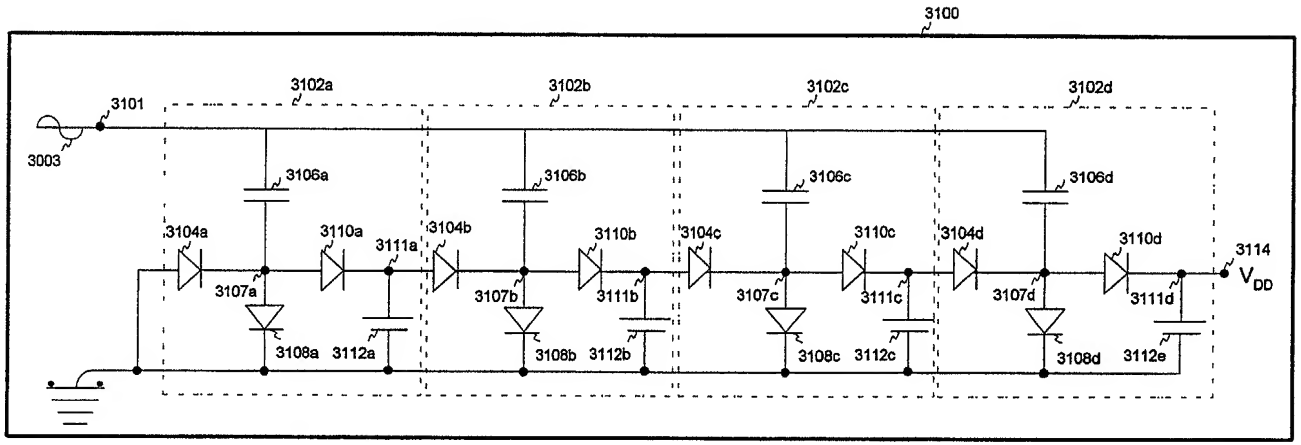
3100
3101
3003
3102a
3102b
3102c
3102d
3106a
3106b
3106c
3106d
3104a
3104b
3104c
3104d
3110a
3110b
3110c
3110d
3111a
3111b
3111c
3111d
3107a
3107b
3107c
3107d
3108a
3108b
3108c
3108d
3112a
3112b
3112c
3112e
3114
V_{DD}

FIG. 31

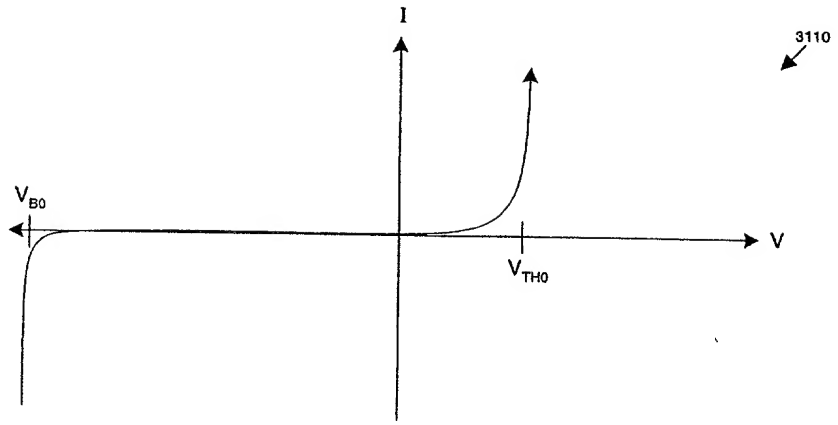

FIG. 32A

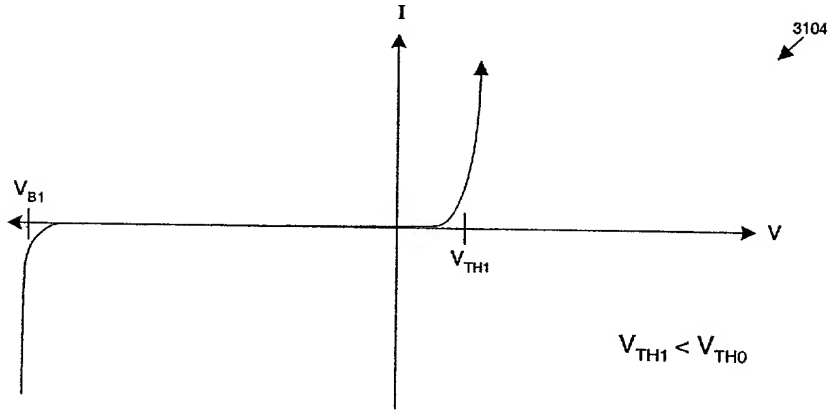

FIG. 32B

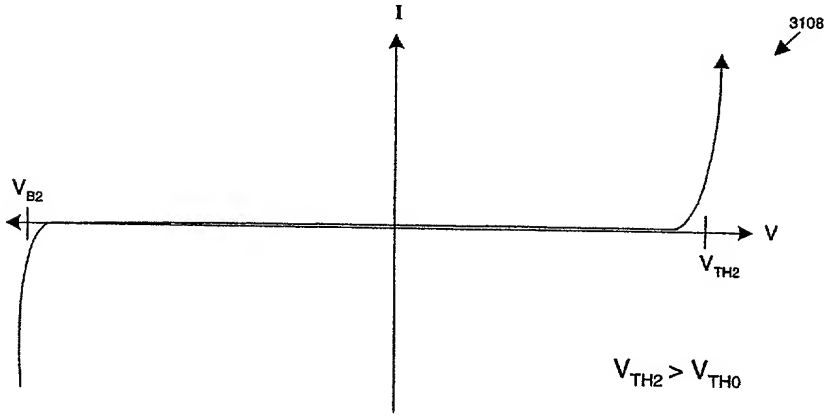

FIG. 32C

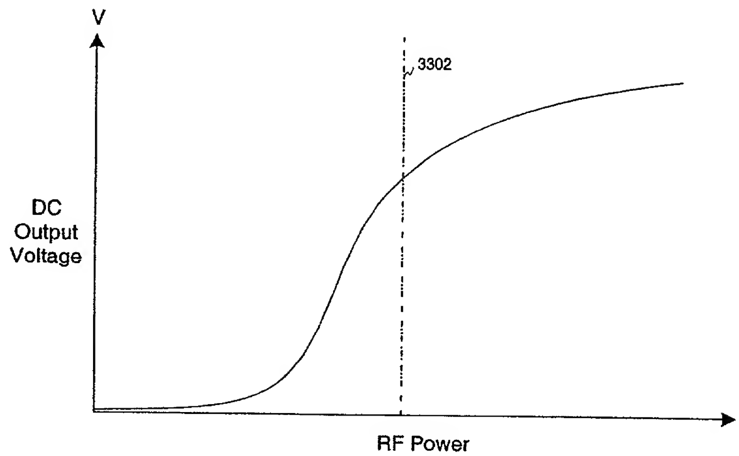

FIG. 33A

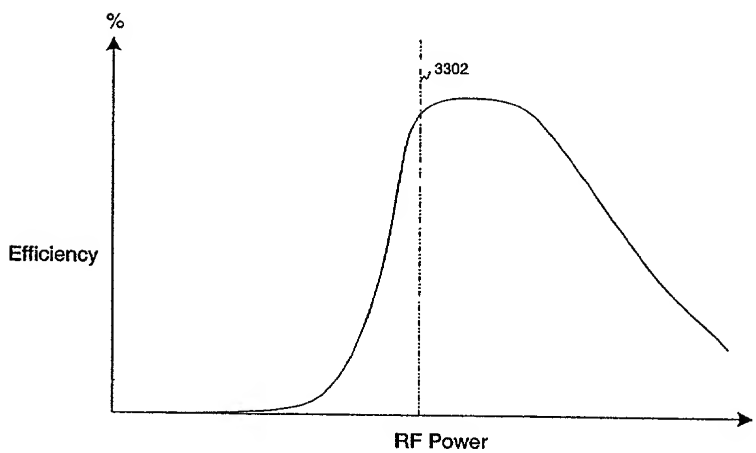

FIG 33B

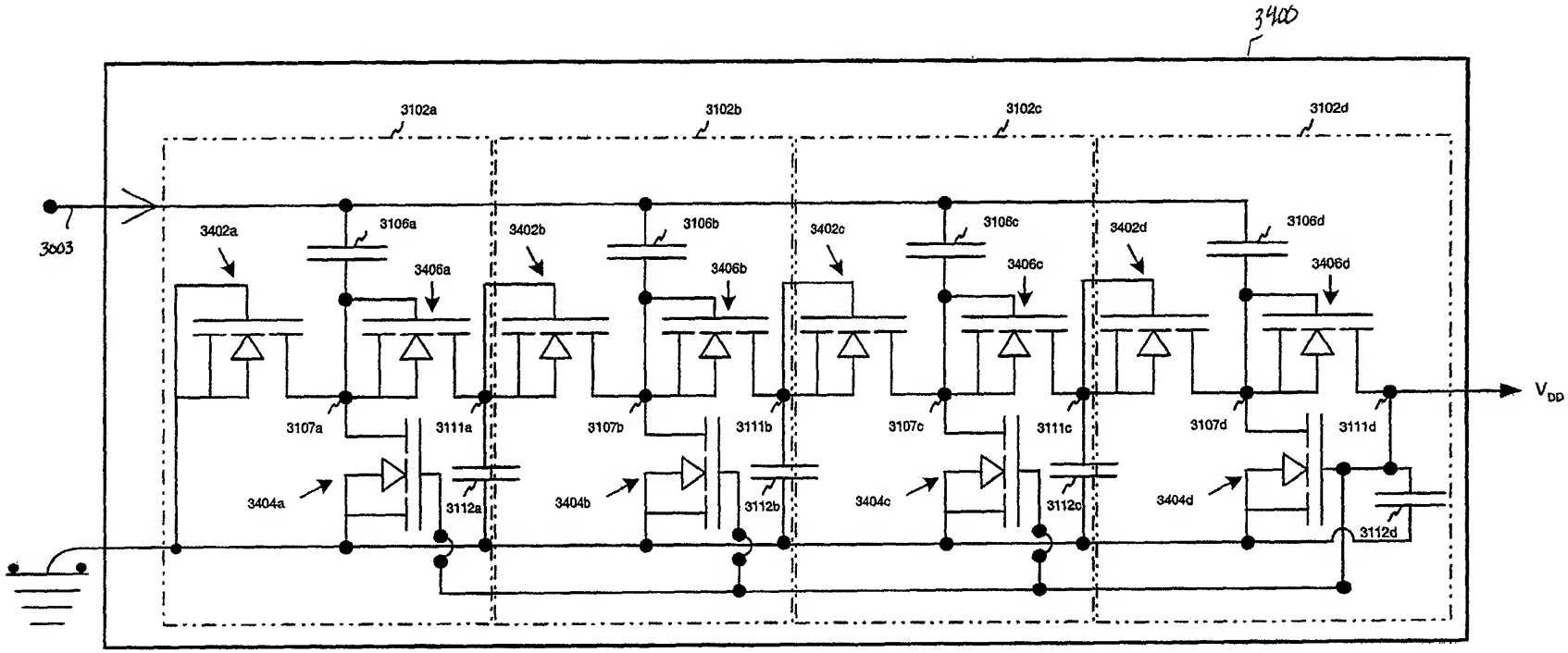
3400
3102a
3102b
3102c
3102d
3603
3402a
3106a
3406a
3402b
3106b
3406b
3402c
3106c
3406c
3402d
3106d
3406d
V_{DD}
3107a
3111a
3107b
3111b
3107c
3111c
3107d
3111d
3404a
3112a
3404b
3112b
3404c
3112c
3404d
3112d

FIG. 34A

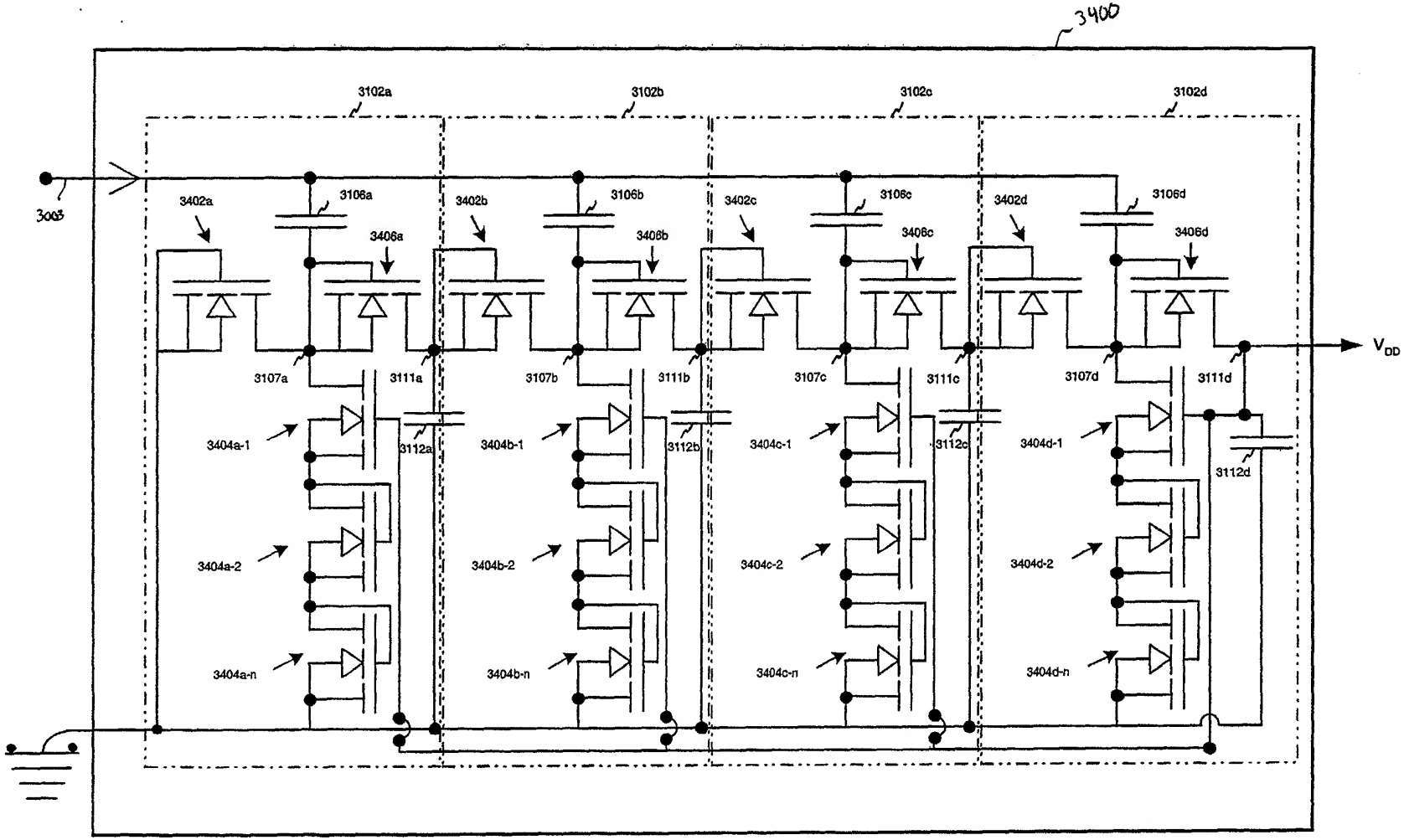
3400
3102a
3102b
3102c
3102d
3003
3402a
3106a
3406a
3402b
3106b
3406b
3402c
3106c
3406c
3402d
3106d
3406d
V_{DD}
3107a
3111a
3107b
3111b
3107c
3111c
3107d
3111d
3404a-1
3112a
3404b-1
3112b
3404c-1
3112c
3404d-1
3112d
3404a-2
3404b-2
3404c-2
3404d-2
3404a-n
3404b-n
3404c-n
3404d-n

FIG. 34B

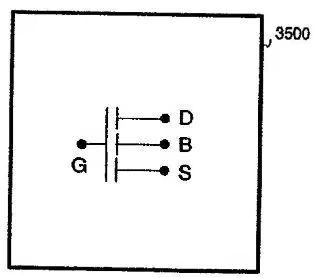

FIG. 35A

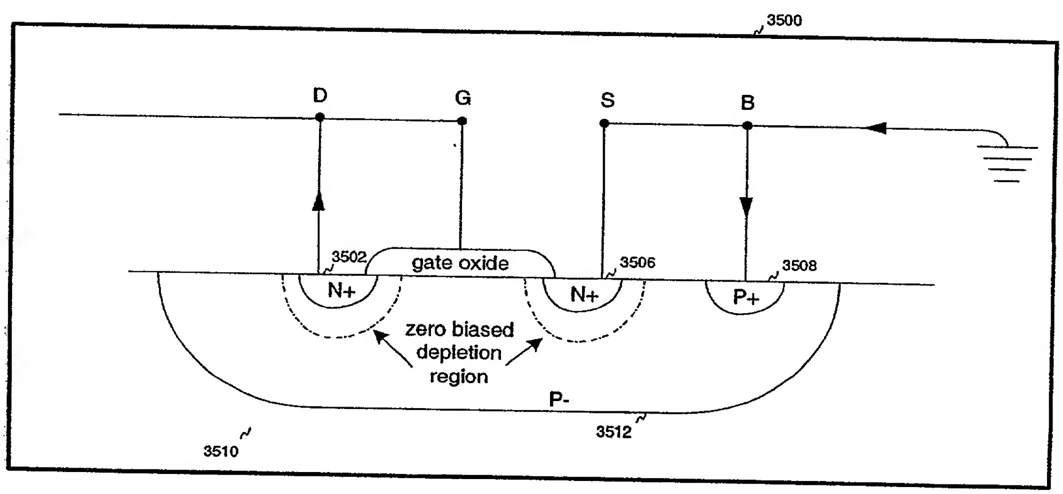

FIG. 35B

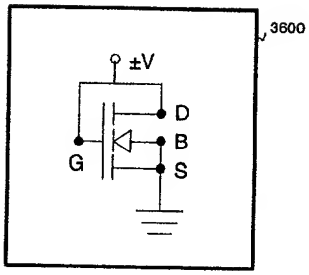

FIG. 36A

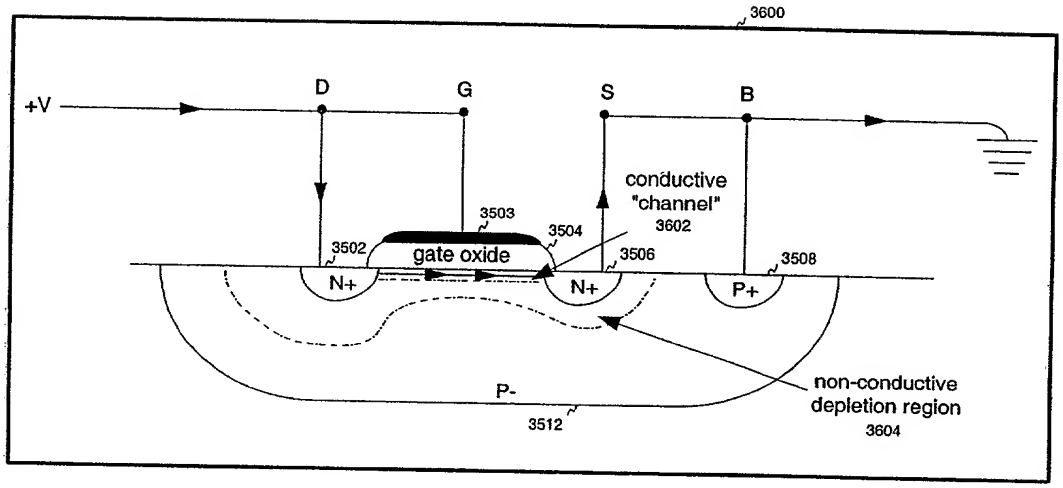

FIG. 36B

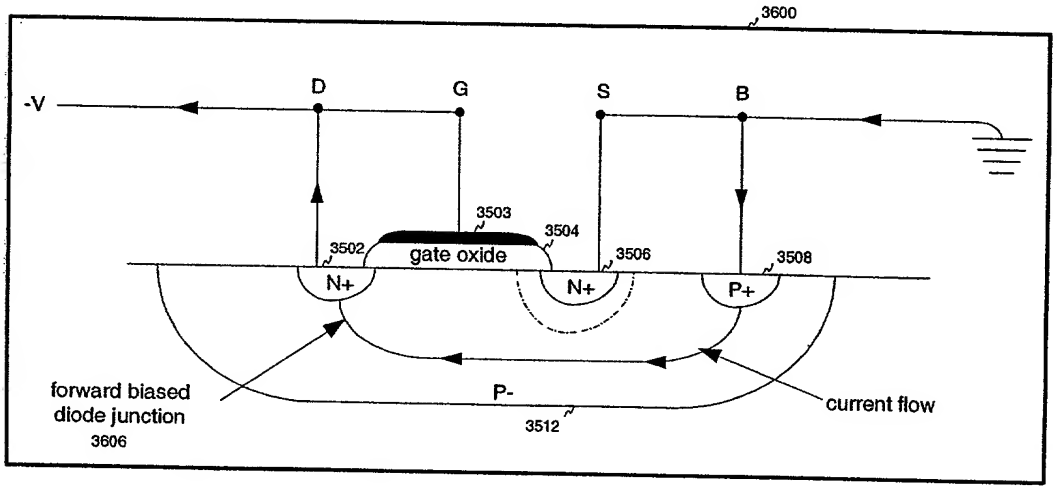

FIG. 36C

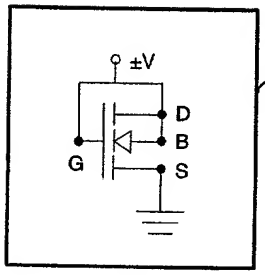

FIG. 37A

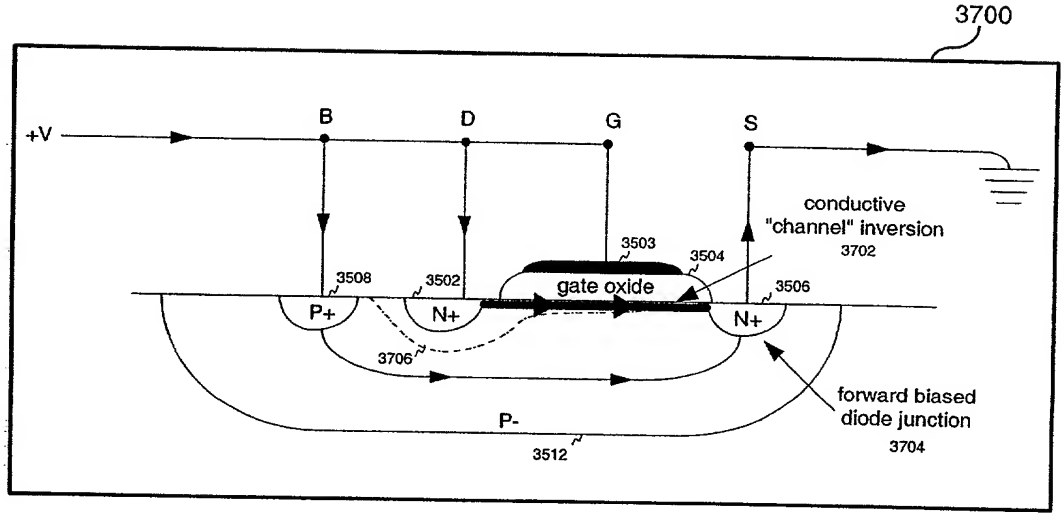

FIG. 37B

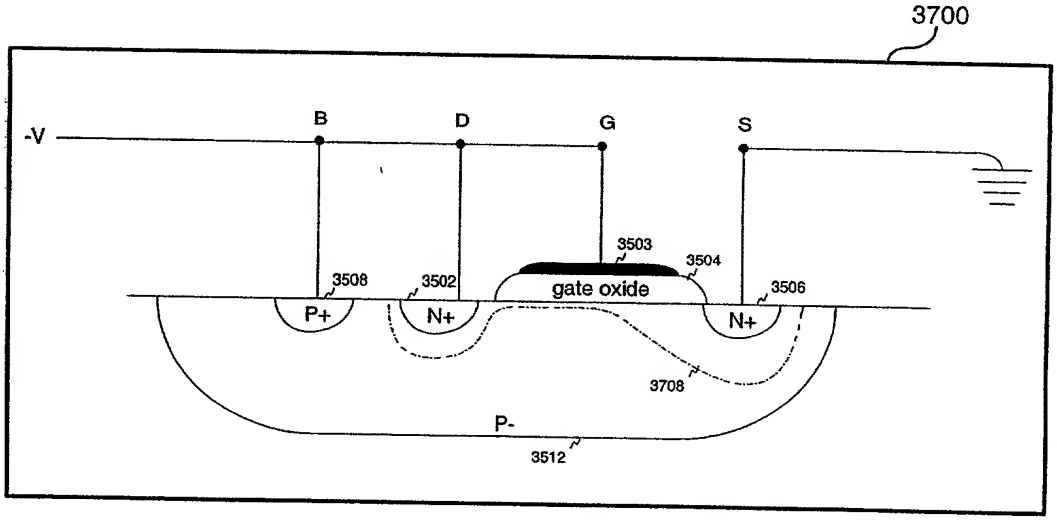

FIG. 37C

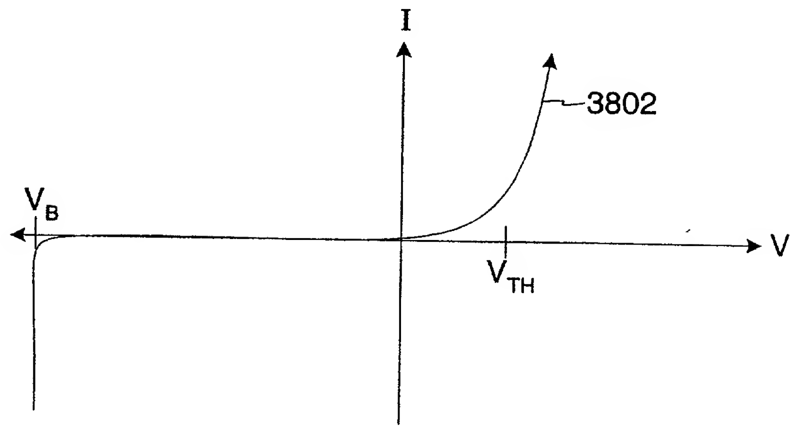

FIG. 38A

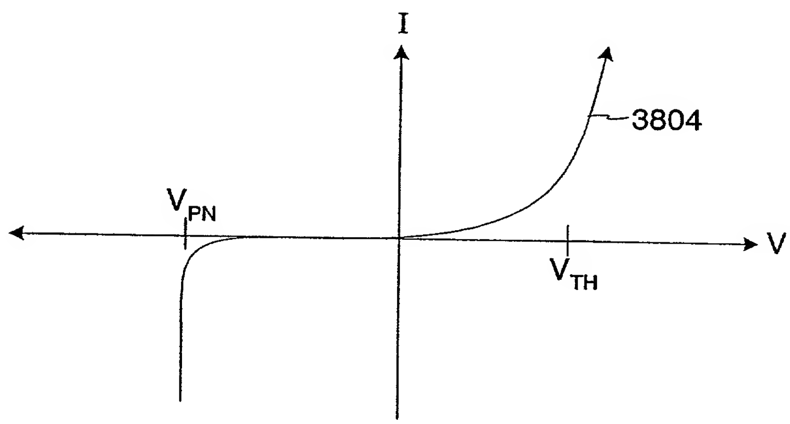

FIG. 38B

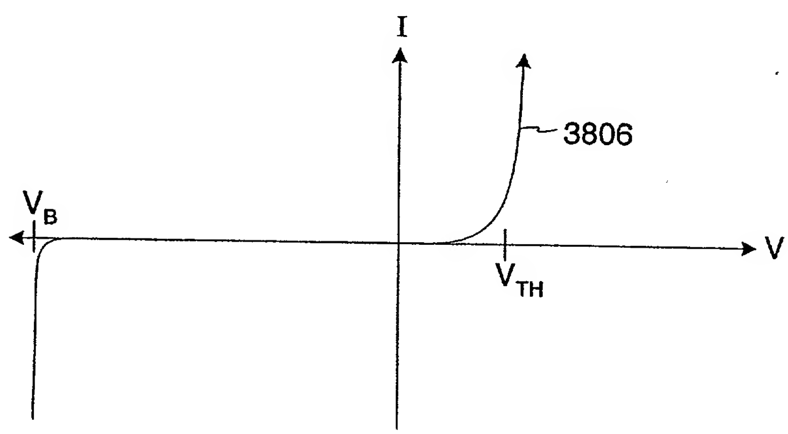

FIG. 38C

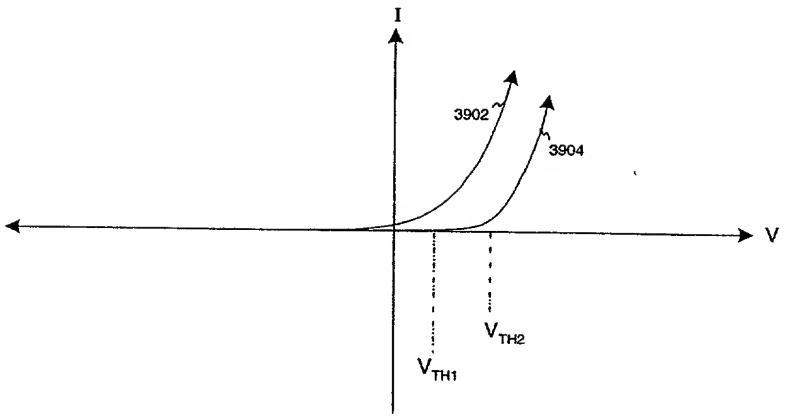

FIG. 39

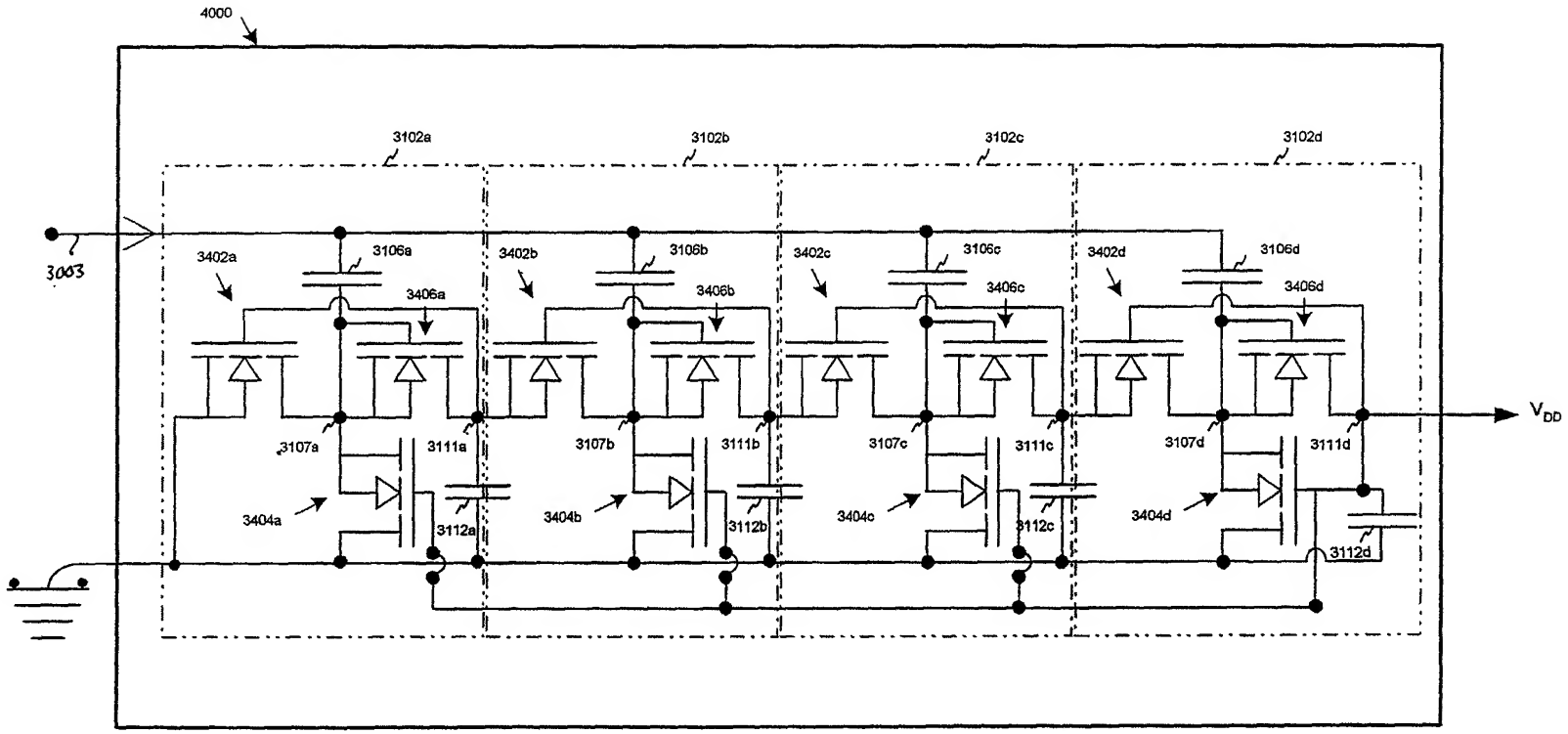

FIG. 40A

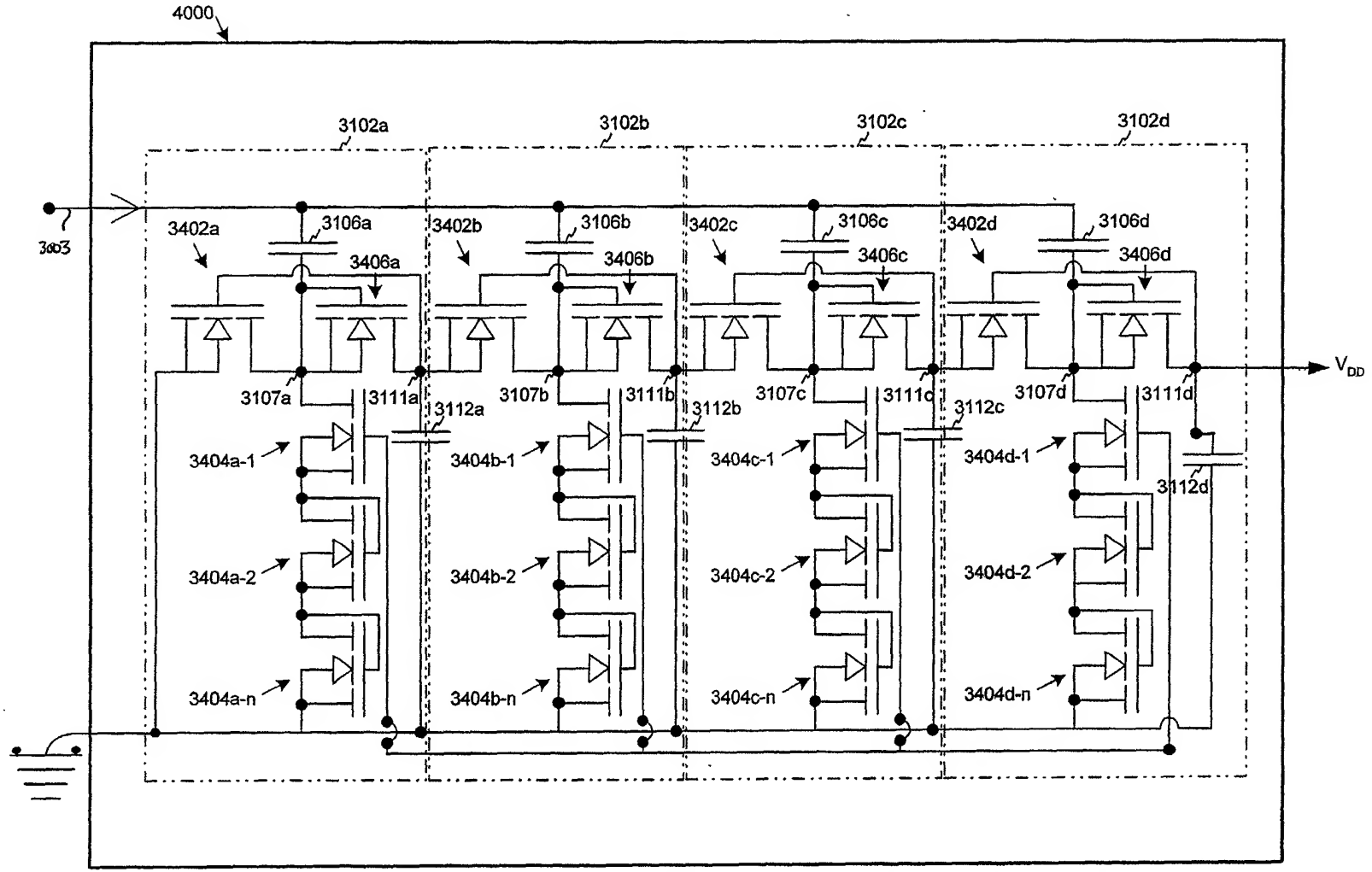
4000
3102a
3102b
3102c
3102d
3303
3402a
3106a
3406a
3402b
3106b
3406b
3402c
3106c
3406c
3402d
3106d
3406d
V_{DD}
3107a
3111a
3112a
3107b
3111b
3112b
3107c
3111c
3112c
3107d
3111d
3112d
3404a-1
3404a-2
3404a-n
3404b-1
3404b-2
3404b-n
3404c-1
3404c-2
3404c-n
3404d-1
3404d-2
3404d-n

FIG. 40B

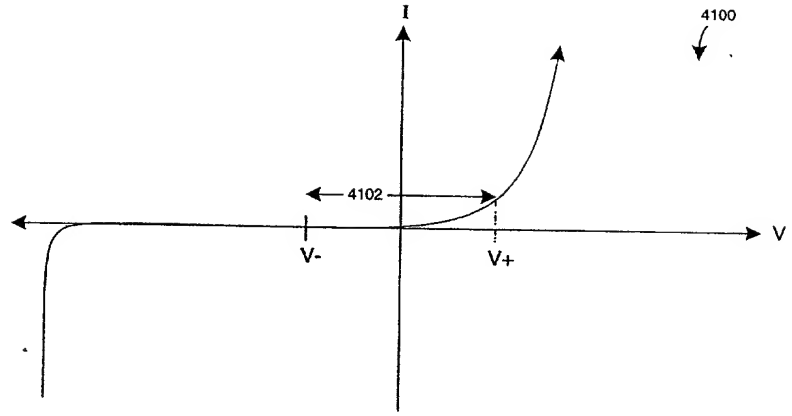

FIG. 41A

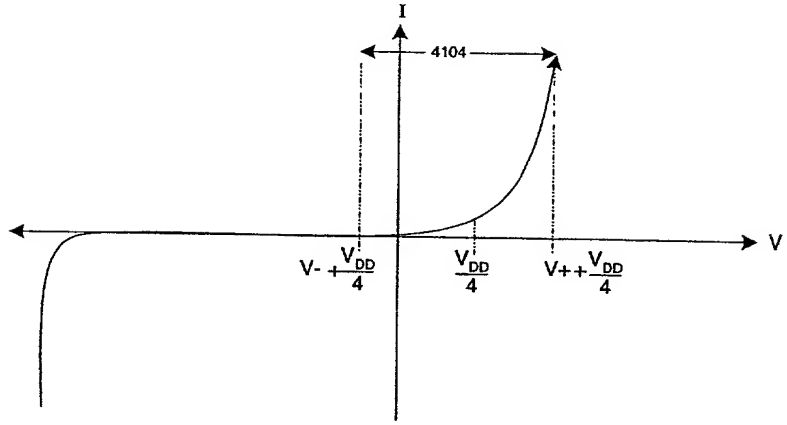

FIG. 41B

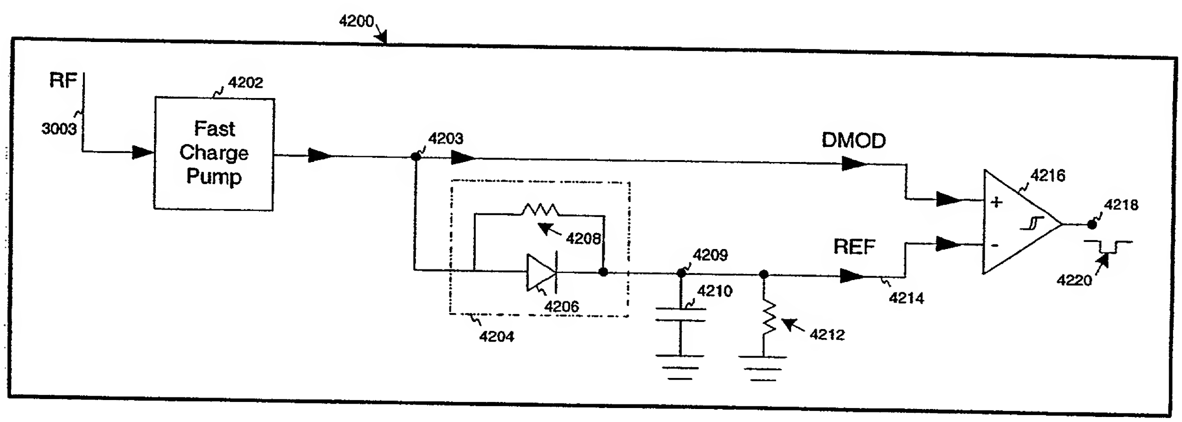
4200
RF
3003
4202
Fast Charge Pump
4203
DMOD
4216
+
-
4218
4208
4209
REF
4210
4206
4214
4220
4204
4212

FIG. 42

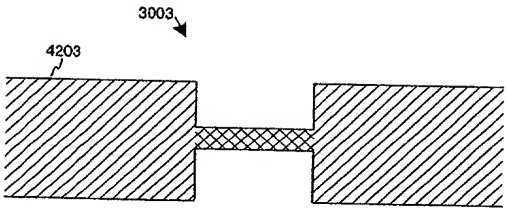

FIG. 43A

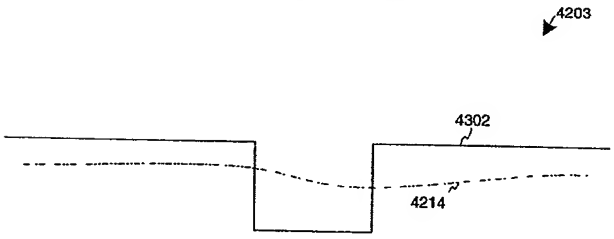

FIG. 43B

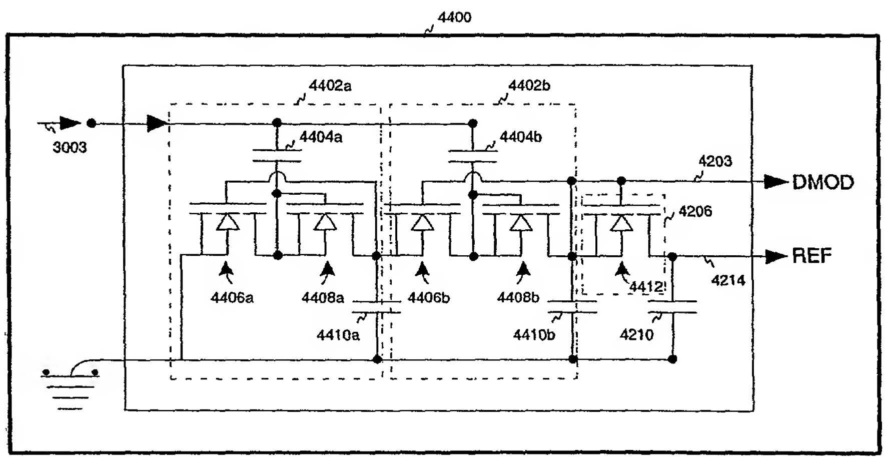

FIG. 44

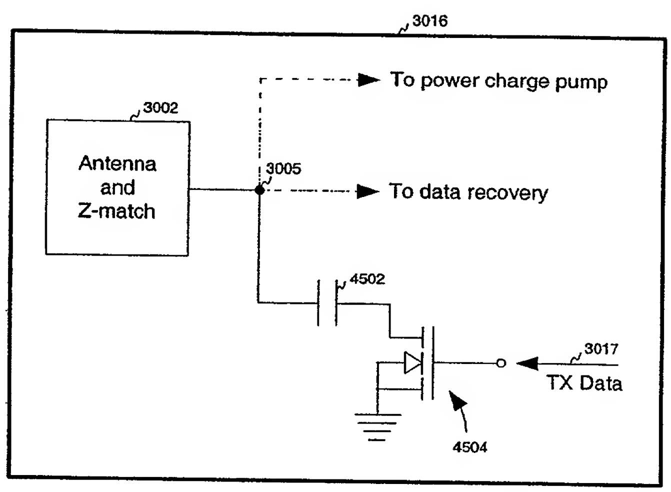
3016
To power charge pump
3002
Antenna
and
Z-match
3005
To data recovery
4502
3017
TX Data
4504

FIG. 45